



## Technical Information

### CCK-MARIMBA

### Mezzanine I/O Expansion Board

### PMC/XMC Module Carrier

Document No. 5098 • Ed. 6 • 26 September 2012



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## About this Manual

This manual is a short form description of the technical aspects of the CCK-MARIMBA, required for installation and system integration. It is intended for the advanced user only.

## Edition History

EKF Document	Ed.	Contents/Changes	Author	Date
Text # 5098 cck_tie.wpd	1	Technical Information CCK-MARIMBA English, preliminary edition	jj	13 March 2008
	2	Added photos	jj	6 January 2009
	3	Added photos top/bottom view	jj	22 October 2009
	4	Added photos CCK-MARIMBA exploded view, added photos C20-SATA	jj	17 November 2009
	5	Added photos CCK-MARIMBA with CCM-BOOGIE CPU carrier card	jj	17 August 2011
	6	Added photo CCK-MARIMBA with DU1-MUSTANG XMC Module	jj	26 September 2012

## Related Documents

For a description of the CCG-RUMBA or CCM-BOOGIE CPU cards, which act as base boards with respect to the CCK-MARIMBA, please refer to the correspondent CPU user guide, available by download from either [www.ekf.com/c/ccpu/ccg/ccg\\_e.html](http://www.ekf.com/c/ccpu/ccg/ccg_e.html) or [www.ekf.com/c/ccpu/ccm/ccm\\_e.html](http://www.ekf.com/c/ccpu/ccm/ccm_e.html).

## Nomenclature

Signal names used herein with an attached '#' designate active low lines.

## Trade Marks

Some terms used herein are property of their respective owners, e.g.

- ▶ Intel, Pentium, Celeron, Pentium M, Core 2 Duo, Merom, Penryn, iAMT: ® Intel
- ▶ Santa Rosa Platform, Crestline Chipset GM965, Matanzas CRB: Intel
- ▶ **CompactPCI**<sup>®</sup>: ® PICMG
- ▶ Windows 2000, Windows XP, Windows Vista: ® Microsoft
- ▶ EKF, ekf system: ® EKF

EKF does not claim this list to be complete.

## Legal Disclaimer - Liability Exclusion

This manual has been edited as carefully as possible. We apologize for any potential mistake. Information provided herein is designated exclusively to the proficient user (system integrator, engineer). EKF can accept no responsibility for any damage caused by the use of this manual.

## Standards

Specifications/Standards	
PMC	IEEE P1386.1
XMC	VITA 42.3
CompactPCI	PICMG 2.0 ( <a href="http://www.picmg.org">www.picmg.org</a> )
PCI Local Bus	PCI 2.2/2.3/3.0 Standards (PCI SIG <a href="http://www.pcisig.com">www.pcisig.com</a> )
PCI Express	PCIe Base Spec. 1.1 and other (PCI SIG <a href="http://www.pcisig.com">www.pcisig.com</a> )
SATA	Serial ATA 2.5/2.6 Specification ( <a href="http://www.sata-io.org">www.sata-io.org</a> )
USB	Universal Serial Bus Revision 2.0 specification ( <a href="http://www.usb.org/developers">www.usb.org/developers</a> )
TPM	Trusted Platform Module 1.2 ( <a href="https://www.trustedcomputinggroup.org">https://www.trustedcomputinggroup.org</a> )

## CCK-MARIMBA Features

Feature Summary	
Form Factor	Single size Eurocard (160x100mm <sup>2</sup> ), needs 4HP (20.3mm) mounting space in addition to CPU carrier board, typically delivered as a ready to use assembly unit (including the CCG-RUMBA or successor CPU card), provided with a common 8HP front panel shared with the CPU board, mounting position right (on top of CPU board)
XMC Module Carrier Function <sup>5</sup>	Carrier for single width XMC mezzanine card (149mm x 74mm) according to VITA 42.0/42.3, connectors J15, J16, suitable for PCIe x 4 (x 1, x 2) XMC modules, J16 may be used for custom specific rear I/O via J1
PMC Module Carrier Function <sup>5</sup>	Carrier for single width PMC mezzanine card (149mm x 74mm) according to IEEE 1386.1, connectors J11, J12, J14, PCI interface 32-bit 33MHz, J14 may be used for custom specific rear I/O via J1
PCIe Packet Switch PCIe Usage	<ul style="list-style-type: none"> <li>▶ PCIe packet switch 3 ports, 4 lanes each (12 lanes in total)</li> <li>▶ 4 Lanes (configured as 1 link x 4 lanes) to host (carrier board ICH)</li> <li>▶ 4 Lanes assigned to XMC module socket J15</li> <li>▶ 1 Lane dedicated to PCIe/PCI bridge (PMC PCI I/F)</li> <li>▶ 1 Lane dedicated to SATA/PATA controller</li> </ul>
SATA/PATA <sup>3</sup>	SMB363 PCIe to 2 x SATA II / 1 x PATA controller, RAID level 0/1 capable
LPC Super-I/O <sup>3</sup> (SIO2)	SCH3114, parallel port, 4 serial ports, PS/2 keyboard & mouse port, GPIO (available via rear I/O J2 connector)
Firmware Hub <sup>3</sup> (FWH2)	82802 generic device, 8Mbit Flash, LPC interface, can be switched as secondary or primary (boot code) FWH
TPM <sup>3</sup>	Option Trusted Platform Module cryptographic chip according to TPM 1.2
Front Panel Connectors	Bezel for PMC/XMC cutout, to be removed when mezzanine module with front panel I/O is inserted
Host I/F Connectors (to CPU Carrier) <sup>1</sup>	<ul style="list-style-type: none"> <li>▶ PCI Express interface (PCIe x 4)</li> <li>▶ Multifunction expansion interface (LPC, USB, SMB)</li> </ul>
On-Board I/O Connectors <sup>1</sup>	<ul style="list-style-type: none"> <li>▶ PMC: J11, J12 - PCI I/F J14 - Rear I/O (to J1)</li> <li>▶ XMC: J15 - PCIe I/F J16 - Rear I/O (to J1)</li> <li>▶ Connector for mounting of optional C20-SATA mezzanine card with 1 or 2 SATA drives 2.5-inch (RAID capable)</li> <li>▶ 2 x Latched SATA headers 7-pos. (option)</li> <li>▶ Socket for C17-CFA CompactFlash mezzanine module (bottom mount)</li> <li>▶ Header suitable for USB Solid State Drive (SSD) module (bottom mount)</li> <li>▶ 2 x Serial port headers (TTL-level)</li> <li>▶ Reset</li> </ul>
Rear I/O Connector Option <sup>1</sup>	Optional J1/J2 2.0mm hard metric connectors (CompactPCI style with proprietary signal mapping) for custom specific transition module or backplane, major signal groups: <ul style="list-style-type: none"> <li>▶ Parallel Port (LPT)</li> <li>▶ COM ports 1 - 4 (TTL-level UART signals)</li> <li>▶ PS/2 keyboard &amp; mouse</li> <li>▶ GPIO</li> <li>▶ SMBus</li> <li>▶ PMC custom specific rear I/O (from J14)</li> <li>▶ XMC custom specific rear I/O (from J16)</li> </ul>
On-Board Functions	Speaker, LEDs, SMBus EEPROM, temperature sensors
Mass Storage Options <sup>2</sup>	<ul style="list-style-type: none"> <li>▶ C20-SATA mezzanine card with 1 or 2 SATA drives 2.5-inch</li> <li>▶ Up to 2 external SATA drives attached to SATA headers</li> <li>▶ C17-CFA (bottom mount) CompactFlash module</li> <li>▶ USB Solid State Drive (SSD) module option (bottom mount)</li> </ul>

Thermal Conditions <sup>4</sup>	<ul style="list-style-type: none"> <li>▶ Operating temperature: 0°C ... +70°C</li> <li>▶ Storage temperature: -40°C ... +85°C, max. gradient 5°C/min</li> <li>▶ Humidity 5% ... 95% RH non condensing</li> </ul>
Environmental Conditions <sup>4</sup>	<ul style="list-style-type: none"> <li>▶ Altitude -300m ... +3000m</li> <li>▶ Shock 15g 0.33ms, 6g 6ms</li> <li>▶ Vibration 1g 5-2000Hz</li> </ul>
EC Regulations	<ul style="list-style-type: none"> <li>▶ EN55022, EN55024, EN60950-1 (UL60950-1/IEC60950-1)</li> <li>▶ 2002/95/EC (RoHS)</li> </ul>
MTBF	tbd

- <sup>1</sup> Not all of these connectors may be present or functional on your actual CCK-MARIMBA board. Assembly of these connectors is highly custom specific. Discuss your needs with EKF before ordering.
- <sup>2</sup> Options may be exclusive, i.e. not necessarily concurrently present. Ask EKF for special solutions if required.
- <sup>3</sup> Silicon/function may not be present on your actual CCK-MARIMBA board. Assembly of components is highly custom specific. Discuss your needs with EKF before ordering.
- <sup>4</sup> Hard disk option may require decrease
- <sup>5</sup> Either one - XMC or PMC module - can be accommodated, exclusively to each other



## Short Description

Available as a mezzanine add-on expansion board to the CCG-RUMBA and successor CPU cards, the CCK-MARIMBA provides a number of additional I/O functions. First of all, the CCK-MARIMBA itself is a carrier board, suitable for accommodation of either a single width PMC or XMC module.

The additional SATA/PATA controller is useful for attachment of mass-storage devices, either on-board mounted, or externally (by cable).

Furthermore the CCK-MARIMBA is equipped with a SIO, which provides legacy I/O ports, such as serial, parallel, KB/MS (all available across rear I/O).

A secondary Firmware Hub can be configured as alternate- or backup-BIOS.

Another option available is the Trusted Platform Module according to TPM 1.2 for safety critical applications.

The CCK-MARIMBA will be attached on top of the CPU carrier board, and typically shares its front panel with the host carrier (usually 8HP front panel width in total). Interconnection between the CCK-MARIMBA I/O module and the CPU carrier board is achieved by two expansion connectors, which comprise the PCIe (PCI Express x 4) and LPC (Low Pin Count) interfaces.

As an option, the CCK-MARIMBA is available with a mezzanine module (C20-SATA), which accommodates one or two 2.5-inch SATA hard disk drives (RAID option). Additionally, a CompactFlash card adapter can be mounted on bottom of the CCK-MARIMBA.



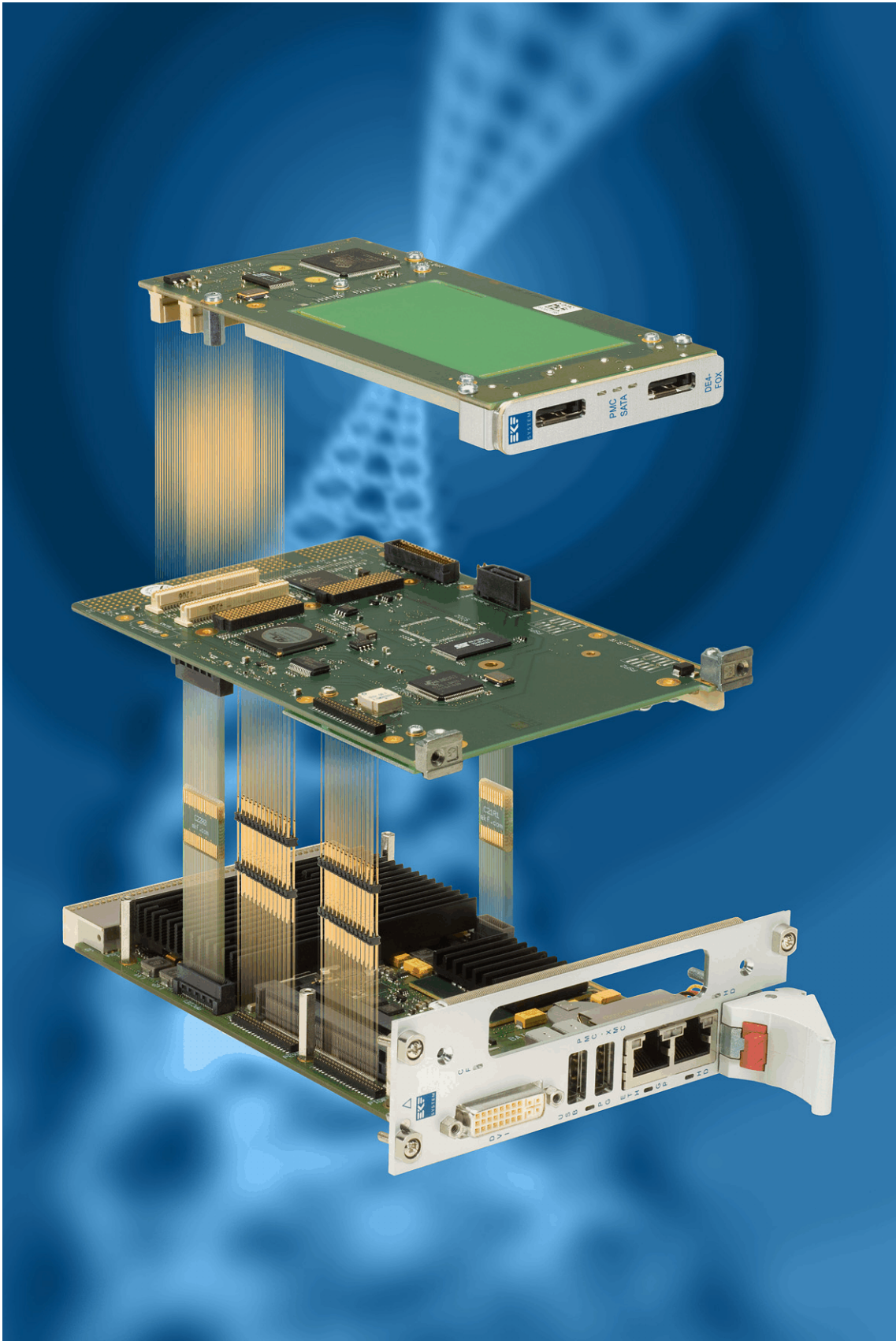
The CCK-MARIMBA communicates by means of 2 bottom mount expansion connectors with the host CPU: P-PCIE (PCI Express x 4), and P-EXP (multi-function I/F such as LPC, USB, SMB).

The PCI Express interface (connector P-PCIE) is comprised of 4 PCIe lanes, which are derived from the ICH (southbridge chip) on the CPU carrier board. All 4 lanes are routed to the primary port of a 3-port 12-lane PCI Express packet switch, which is the main component of the CCK-MARIMBA.

Connector P-EXP combines several other southbridge data channels: The LPC (Low Pin Count) is a multiplexed ISA bus, e.g. enabling the super-I/O (SIO) controller chip to emulate the legacy I/O interfaces; among these are the classic parallel (printer) and serial (COM) ports. Two USB channels are provided, one for the optional USB SSD, and one or both for rear I/O via the J2 connector.

The Trusted Platform Module is an optionally available cryptographic chip, which provides a comprehensive hardware and software solution for safer computing. Conforming to the TPM1.2 standard of the TCG, the TPM is comprised of a 16-bit security controller and additional hardware e.g. to generate 2048 bit RSA keys and true random numbers, thus meeting the highest industry rating for digital security.

The CCK-MARIMBA fits on the top side of the CPU board, which is on the right side when viewing the common front panel. A suitable backplane provides its CPCI slots beginning with the CPU carrier board (CPCI system slot) from right to left. The CPCI system must provide additional mounting space to the right side for the CCK-MARIMBA. In addition, a single slot rear I/O backplane would be needed for rear I/O usage, and a custom specific rear I/O transition module.



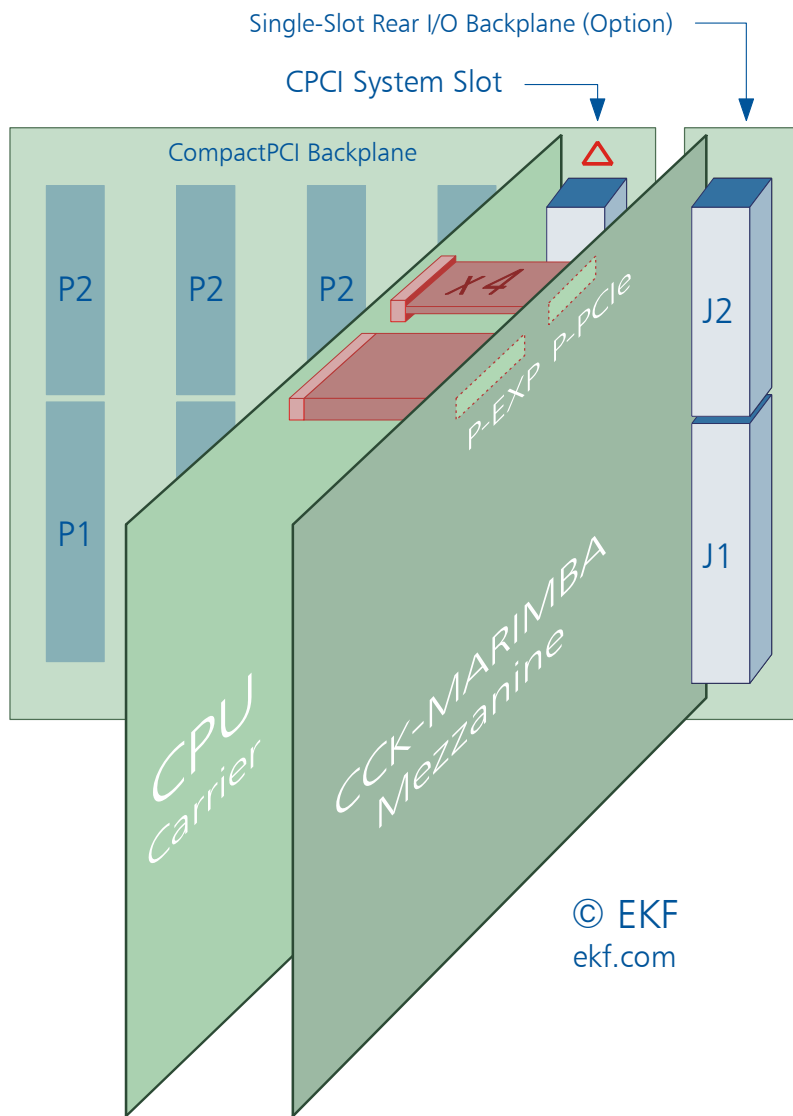
CPU Board • PMC/XMC Carrier Side Card • DE1-FOX PMC Module



CPU Board • PMC/XMC Carrier Side Card • DX1-LYNX XMC Module (Dual Drive)



CPU Board • PMC/XMC Carrier Side Card • DU1-MUSTANG XMC Module



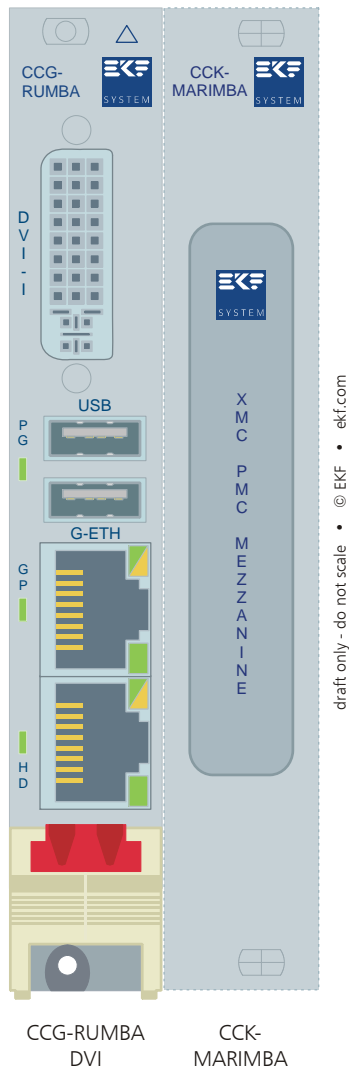
CCK-MARIMBA on Top of the CPU Carrier

As of current, the suitable CPU carrier board for use together with the CCK-MARIMBA mezzanine module is the CCG-RUMBA (successor CCM-BOOGIE available late 2008). The CCK-MARIMBA expansion board mounts on top (at the right side) of the CCG-RUMBA.

If the CompactPCI backplane is provided with a right aligned system slot, be sure to position the CPU carrier board to the rightmost CPCI slot (and not the CCK-MARIMBA). Consequently, the CCK-MARIMBA then occupies the next card slot to the right, outside of the CPCI backplane, which may be provided with a single slot rear I/O P1/P2 backplane. In order to make use of the rear I/O capability of the CCK-MARIMBA, its optional J1/J2 rear I/O connectors must be stuffed (consider before ordering). This assembly order (right aligned CPCI system slot) is preferred because no CompactPCI slot is lost in a system for the CCK-MARIMBA.

Vice versa, if a CPCI backplane is mandatory with a left aligned system slot, the CCK-MARIMBA must not be equipped with J1/J2 connectors, and occupies a regular CompactPCI slot then. Of course, this assembly solution is not suitable for rear I/O with the CCK-MARIMBA, and a CPCI slot will be lost. With J1/J2 stuffed, a coding key present on J1 would prevent insertion of the CCK-MARIMBA into a CPCI card slot.

## Front Panel

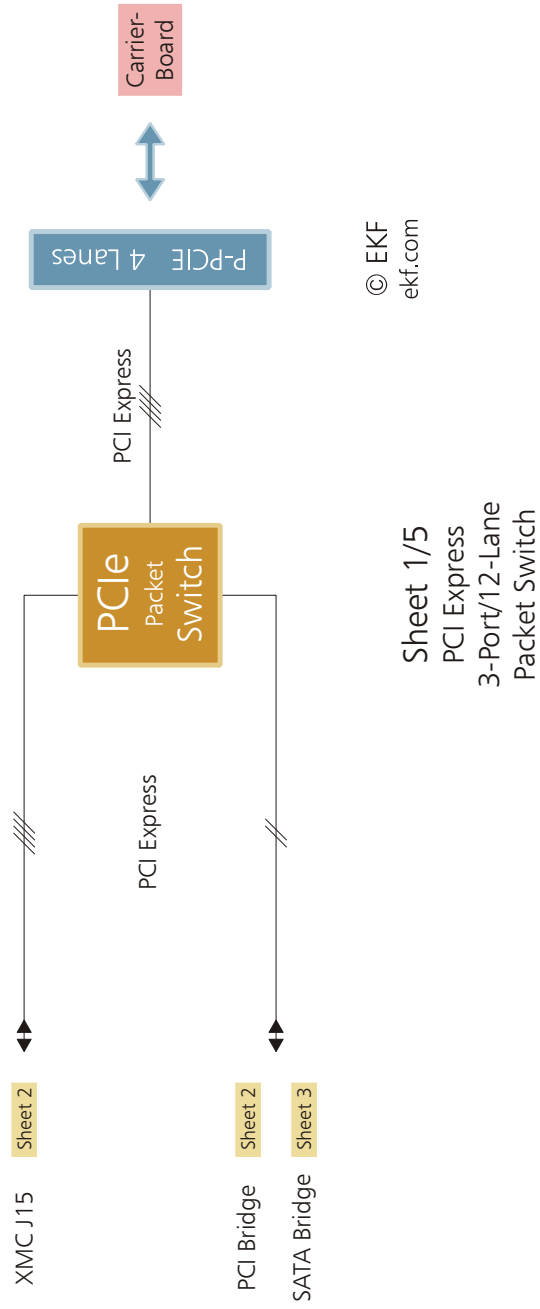


Typically the CCG-RUMBA carrier board CPU and the CCK-MARIMBA share a common 3U/8HP front panel. Not shown in the illustration above are variations of the CCG-RUMBA (e.g. with VGA connector rather than DVI).

There may be reasons for further widening of the front panel (e.g. 12HP width); this would provide additional space e.g. for serial port connectors (CU-series modules). Please discuss your needs for an individual solution with EKF.

Block Diagram

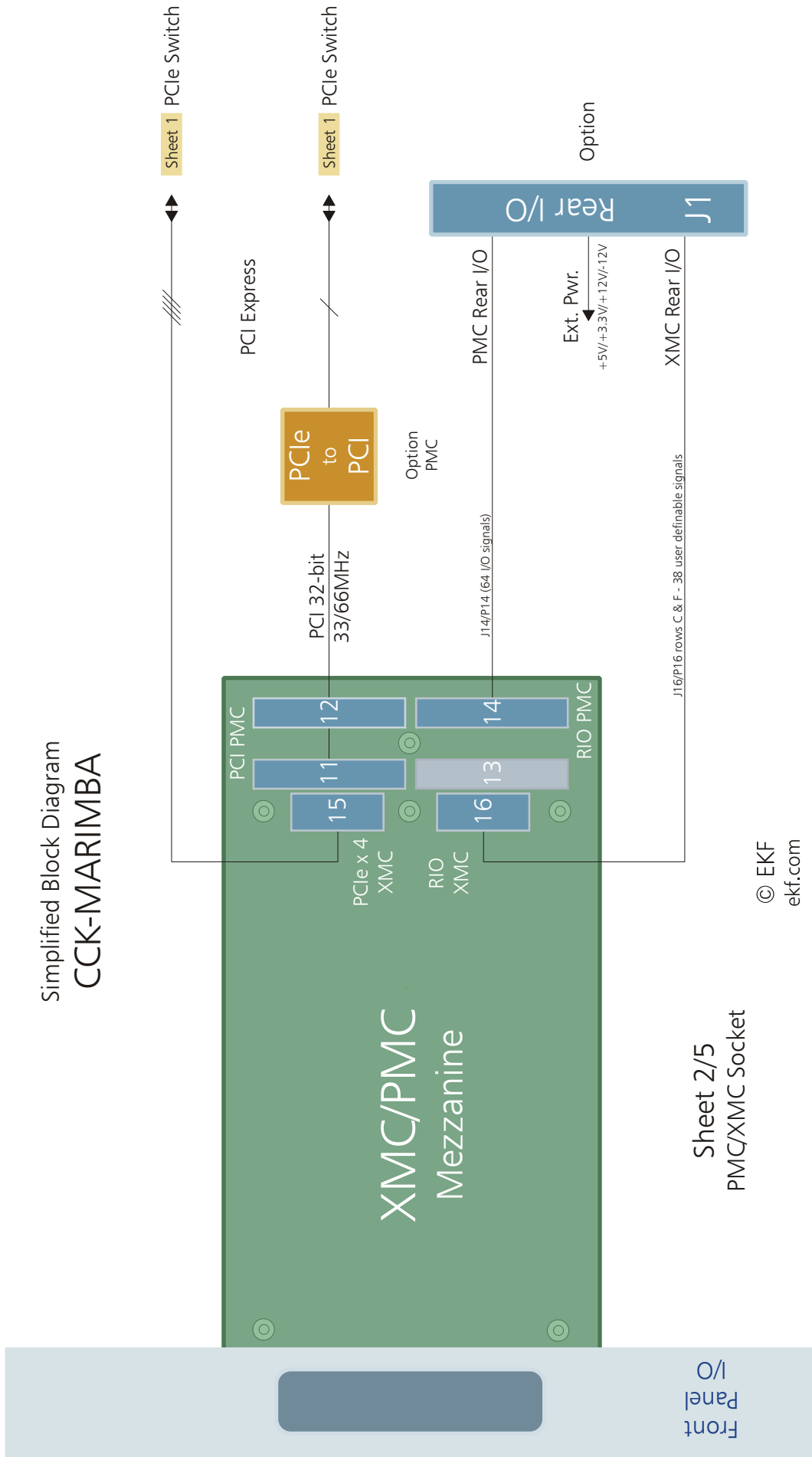
Simplified Block Diagram  
CCK-MARIMBA

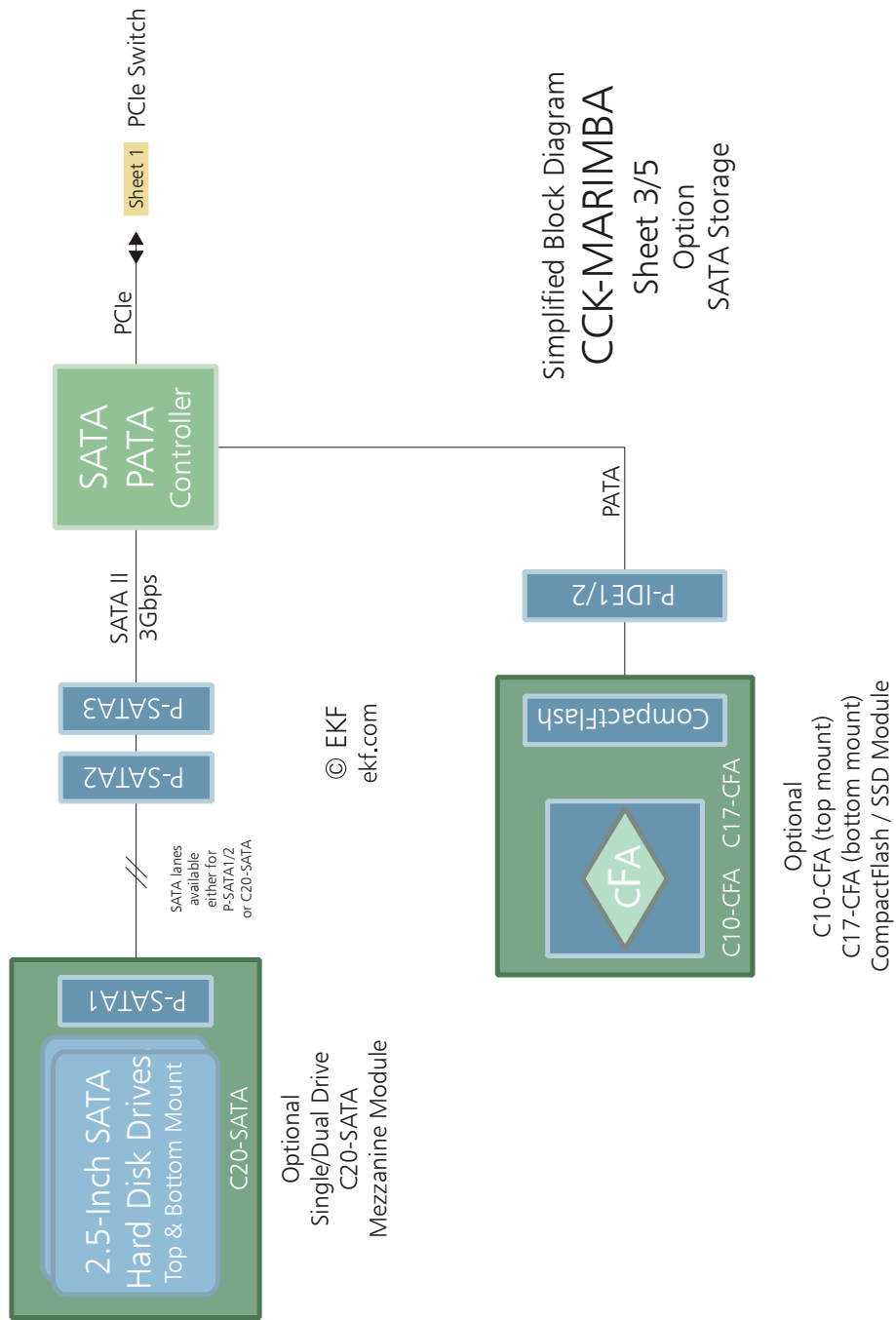


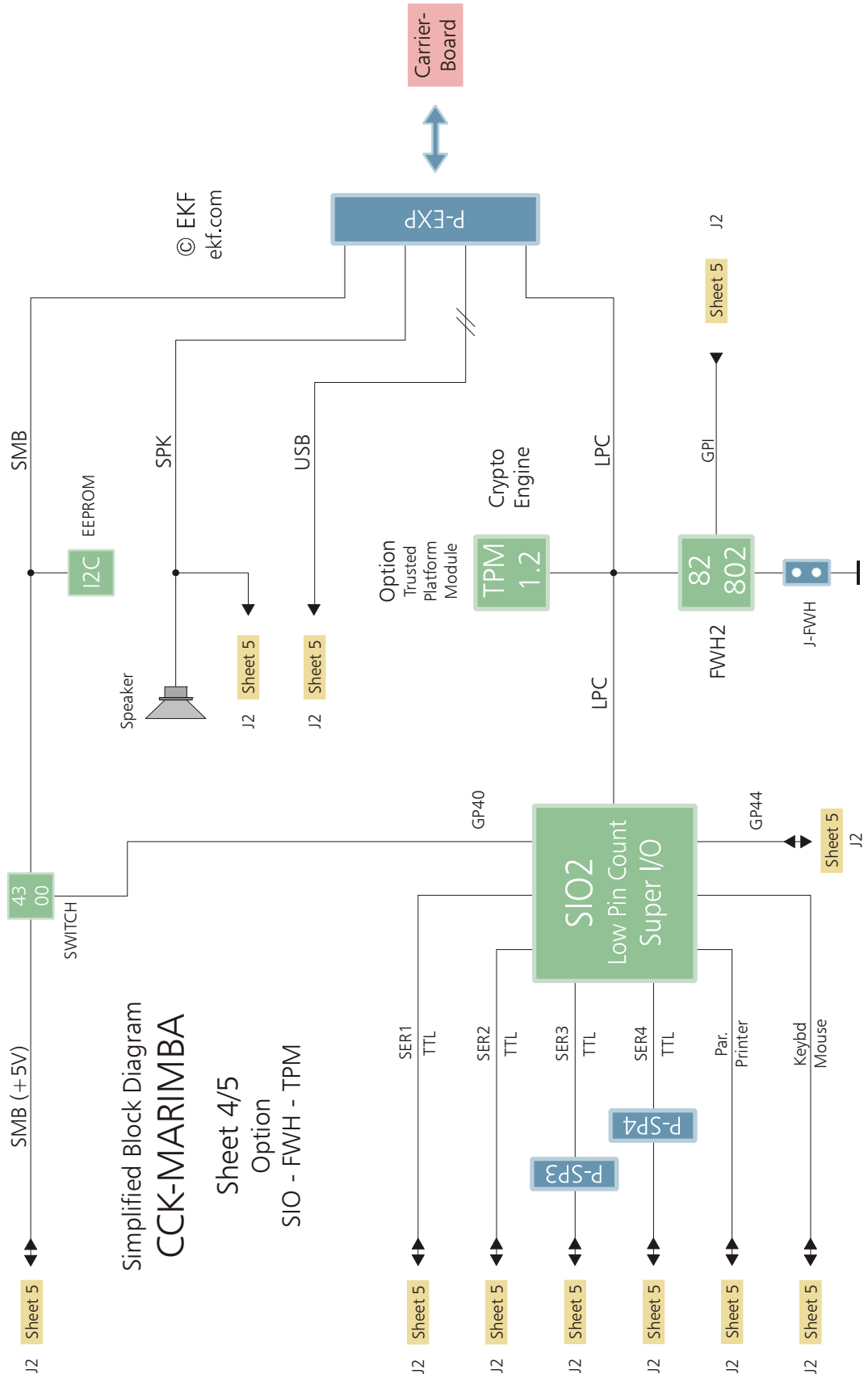
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Sheet 1/5  
PCI Express  
3-Port/12-Lane  
Packet Switch





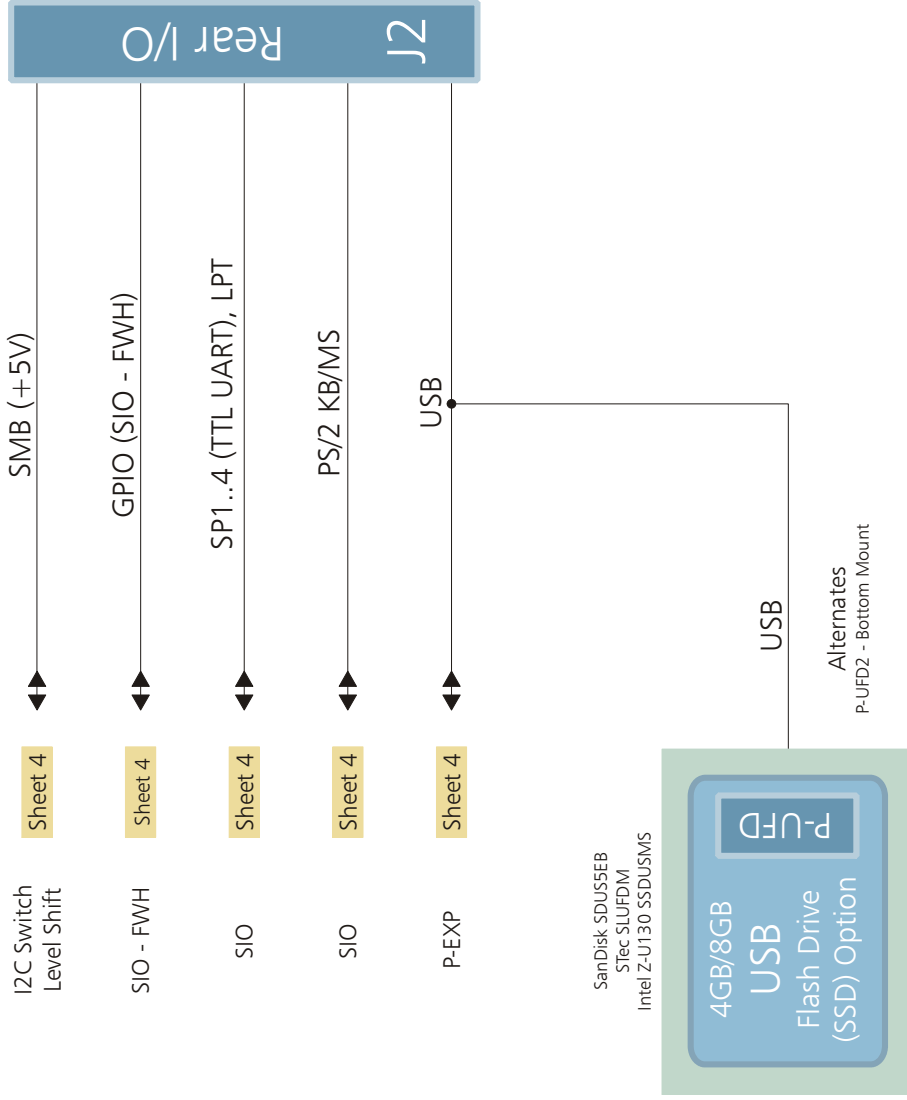




Simplified Block Diagram  
CCK-MARIMBA

Sheet 4/5  
Option  
SIO - FWH - TPM

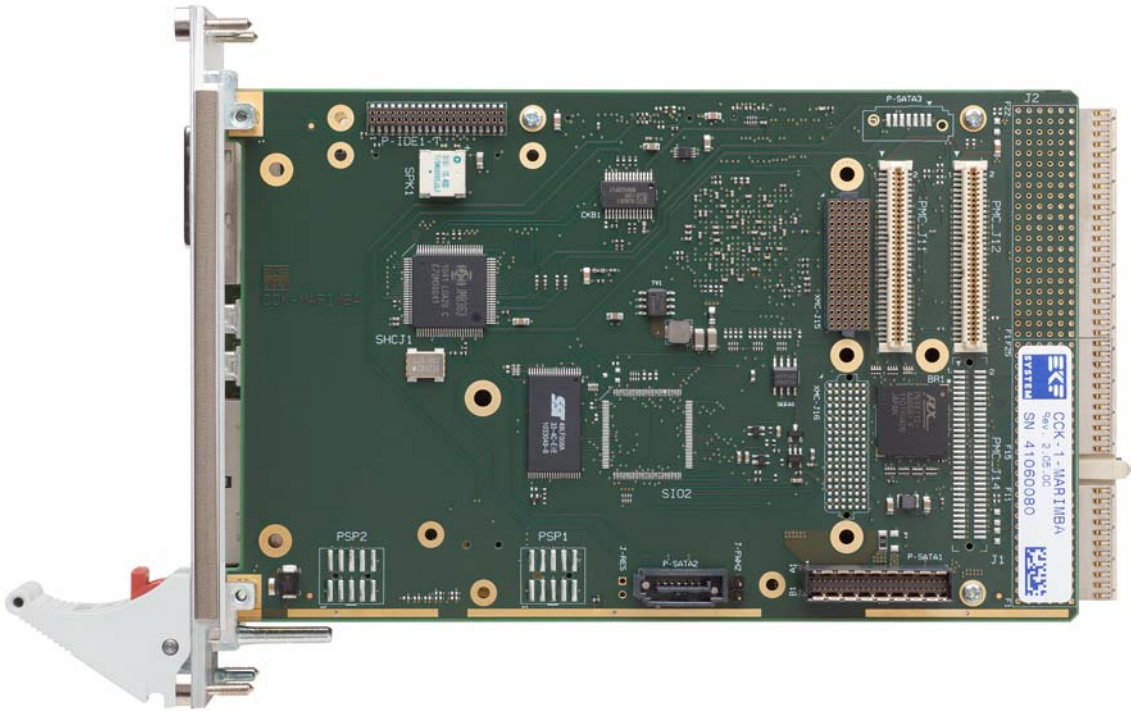
# Simplified Block Diagram CCK-MARIMBA



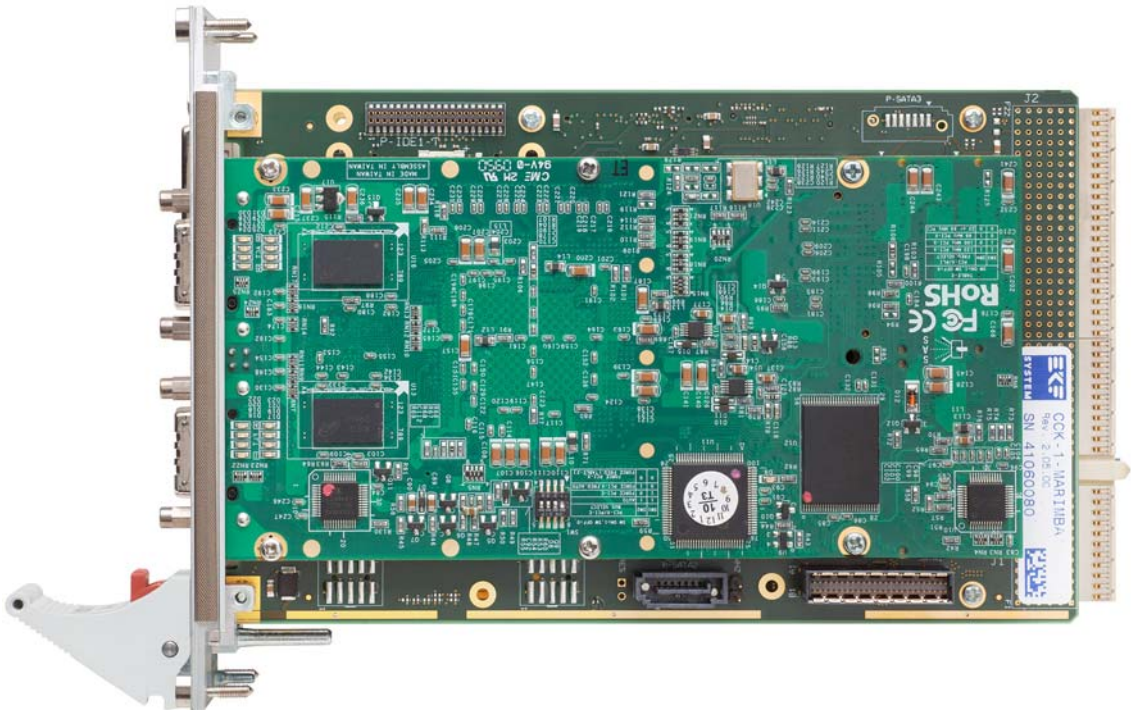
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Sheet 5/5  
J2 Rear I/O  
Option

Top View



Assembly w/o PMC/XMC Module



Assembly with PMC/XMC Module

## On-Board Connectors

J11, J12	PMC module, PCI interface
J14	PMC module, rear I/O option
J15	XMC module, PCI Express interface
J16	XMC module, rear I/O option
P-IDE2	PATA socket (bottom mount), suitable for C17-CFA CompactFlash module
P-SATA1	Microspeed female connector, for top mount attachment of a C20-SATA mezzanine module, equipped with either one or two SATA drives 2.5-inch (RAID option with 2 drives)
P-SATA2 P-SATA3	Vertical latched SATA header, 7-position, stuffing option (exclusive to P-SATA1)
P-SP3 <sup>1</sup> P-SP4	Pin headers 10-lead 2.00mm, provide TTL level serial COM port signals (CU-series modules)
P-UFD2 <sup>2</sup>	Socket (bottom mount) 10-lead 2.00mm pitch, for low profile USB SSD (Solid State Drive)

<sup>1</sup> Due to a primary SIO which may be present on the CPU board itself, the BIOS may assign COM port numbers different from COM3/COM4 to these interface lines on the CCK-MARIMBA, e.g. COM4/COM5.

<sup>2</sup> USB channel shared (stuffing option) with J2 for rear I/O

## Jumpers

J-FWH <sup>1</sup>	Jumper 2.54mm, determines if the optional on-board firmware hub is acting as boot BIOS (jumper set) or as secondary BIOS (jumper removed = default).
J-RES <sup>1</sup>	Jumper 2.54mm, allows to force a CPU debug reset on the CCG-RUMBA CPU carrier board

<sup>1</sup> Not all of these jumpers may be present or functional on your actual CCK-MARIMBA board. Assembly of these jumpers is highly custom specific. Discuss your needs with EKF before ordering.

## Inter-Board Connectors

P-EXP	Dual row socket, available from bottom of the CCK-MARIMBA PCB, matching with the corresponding socket on the CPU carrier board, connected through a board stacker, comprising of: <ul style="list-style-type: none"> <li>• LPC Low Pin Count interface</li> <li>• AC'97 Audio Codec / HD Audio (Azalia)</li> <li>• 2 x USB</li> <li>• SMB, Speaker, Reset</li> </ul>
P-PCIE	High speed socket edge card connector, available from bottom of the CCK-MARIMBA PCB, matching with the corresponding socket on the CPU carrier board, connected through a high speed strip line PCB (C22), comprising of: <ul style="list-style-type: none"> <li>• Host CPU (ICH8) PCI Express (PCIe) x 4 interface</li> </ul>

## Rear I/O Connectors

J1 <sup>2</sup>	2.00mm brown keyed Hard Metric female connector, signal groups PMC rear I/O, XMC rear I/O
J2 <sup>2</sup>	2.00mm Hard Metric female connector, signal groups GPIO, parallel port, serial ports (TTL-level signals), USB, SMB (+5V), speaker

<sup>2</sup> J1/J2 are optional

Please note:

Not all of the connectors or other elements listed above may be present or functional on your actual CCK-MARIMBA board. Assembly of these connectors is highly custom specific. Discuss your needs (target application) with EKF before ordering, for an optimum board configuration.

## Installing and Replacing Components

### Before You Begin

#### Warnings

The procedures in this chapter assume familiarity with the general terminology associated with industrial electronics and with safety practices and regulatory compliance required for using and modifying electronic equipment. Disconnect any telecommunication links, networks or procedures described in this chapter. Failure links before you open the system or perform or equipment damage. Some parts of the the power switch is in its off state.



the system from its power source and from modems before performing any of the to disconnect power, or telecommunication any procedures can result in personal injury system can continue to operate even though

#### Caution

Electrostatic discharge (ESD) can damage components. Perform the procedures described in this chapter only at an ESD workstation. If such a some ESD protection by wearing an metal part of the system chassis or board original ESD protected packaging. Retain the antistatic box) in case of returning the board to EKF for repair.



station is not available, you can provide antistatic wrist strap and attaching it to a front panel. Store the board only in its original packaging (antistatic bag and



## Installing the Board

### Warning

This procedure should be done only by qualified technical personnel. Disconnect the system from its power source before doing the procedures described here. Failure to disconnect power, or telecommunication links before you open the system or perform any procedures can result in personal injury or equipment damage.

Typically you will perform the following steps:

- Switch off the system, remove the AC power cord
- Attach your antistatic wrist strap to a metallic part of the system
- Remove the board packaging, be sure to touch the board only at the front panel
- Identify the related CompactPCI slot (peripheral slot for I/O boards, system slot for CPU boards, with the system slot typically most right or most left to the backplane)
- Insert card carefully (be sure not to damage components mounted on the bottom side of the board by scratching neighbored front panels)
- A card with onboard connectors requires attachment of associated cabling now
- Lock the ejector lever, fix screws at the front panel (top/bottom)
- Retain original packaging in case of return



## Removing the Board

### Warning

This procedure should be done only by qualified technical personnel. Disconnect the system from its power source before doing the procedures described here. Failure to disconnect power, or telecommunication links before you open the system or perform any procedures can result in personal injury or equipment damage.

Typically you will perform the following steps:

- Switch off the system, remove the AC power cord
- Attach your antistatic wrist strap to a metallic part of the system
- Identify the board, be sure to touch the board only at the front panel
- unfasten both front panel screws (top/bottom), unlock the ejector lever
- Remove any onboard cabling assembly
- Activate the ejector lever
- Remove the card carefully (be sure not to damage components mounted on the bottom side of the board by scratching neighbored front panels)
- Store board in the original packaging, do not touch any components, hold the board at the front panel only



### Warning

Do not expose the card to fire. Battery cells and other components could explode and cause personal injury.





## EMC Recommendations

In order to comply with the CE regulations for EMC, it is mandatory to observe the following rules:

- The chassis or rack including other boards in use must comply entirely with CE
- Close all board slots not in use with a blind front panel
- Front panels must be fastened by built-in screws
- Cover any unused front panel mounted connector with a shielding cap
- External communications cable assemblies must be shielded (shield connected only at one end of the cable)
- Use ferrite beads for cabling wherever appropriate
- Some connectors may require additional isolating parts

## Reccomended Accessories

Blind CPCI Front Panels	EKF Elektronik	Widths currently available (1HP=5.08mm): with handle 4HP/8HP without handle 2HP/4HP/8HP/10HP/12HP
Ferrit Bead Filters	ARP Datacom, 63115 Dietzenbach	Ordering No. 102 820 (cable diameter 6.5mm) 102 821 (cable diameter 10.0mm) 102 822 (cable diameter 13.0mm)
Metal Shielding Caps	Conec-Polytronic, 59557 Lippstadt	Ordering No. CDFA 09 165 X 13129 X (DB9) CDSFA 15 165 X 12979 X (DB15) CDSFA 25 165 X 12989 X (DB25)

## Technical Reference - Connectors

### Caution

Some of the connectors may provide operating voltage (e.g. +12V, +5V and +3.3V) to devices inside the system chassis, such as internal peripherals. Not all of these connectors are overcurrent protected. Do not use these connectors for powering devices external to the computer chassis. A fault in the load presented by the external devices could cause damage to the board, the interconnecting cable and the external devices themselves.

### Please Note

The CCK-MARIMBA mezzanine module may be equipped with several on-board connectors for system internal usage. Not all of these connectors may be present on a particular board. Be sure to specify your individual needs when ordering the CCK-MARIMBA board. Characteristic features and the pin assignments of each connector are described on the following pages (connector designation in alphabetical order within the groups 'on-board connectors', 'inter-board connectors', and 'rear I/O connectors').

## On-Board Connectors

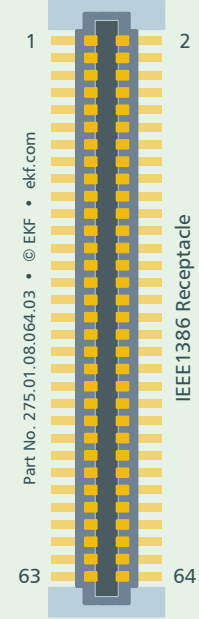
The CCK-MARIMBA can be equipped with several on-board connectors. Some of these connectors are available as an option only or exclusive to each other, and therefore may not be functional or even present on your actual board.

Assembly of these connectors is highly custom specific. Discuss your needs with EKF before ordering, so that the optimum board configuration for your application will be chosen.

## PMC Socket Receptacles J11 J12 J14

The CCK-MARIMBA is a PMC carrier board with 32-bit PCI host interface. Hence, 3 (of max. 4) IEEE P.1386 PMC connectors are provided, PMC-J11, -J12 and -J14. There is no need for -J13 which would be a requirement for 64-bit PCI only. The 32-bit PCI interface is comprised of PMC-J11 and -J12, while PMC-J14 is reserved for optional rear I/O usage across the connector J1 (custom specific rear I/O transition module). A custom specific rear I/O transition module can be discussed with EKF (sales@ekf.de).

The PMC module PCI host interface is provided by the PCI Express to PCI bridge PEX8112, which is connected to the PCI Express packet switch. The PCI interface VIO voltage is set to +3.3V by default. If required, +5V is also available as PCI VIO, by means of a stuffing option.

PMC-J11 - PCI				
	1	<i>TCK</i>	-12V <sup>4)</sup>	2
	3	GND	INTA#	4
	5	INTB#	INTC#	6
	7	BUSMODE1# <sup>1)</sup>	+5V	8
	9	INTD#	<i>Reserved</i>	10
	11	GND	+3.3V (+3.3Vaux)	12
	13	CLK	GND	14
	15	GND	GNT#	16
	17	REQ#	+5V	18
	19	VI/O <sup>3)</sup>	AD31	20
	21	AD28	AD27	22
	23	AD25	GND	24
	25	GND	C/BE3#	26
	27	AD22	AD21	28
	29	AD19	+5V	30
	31	VI/O <sup>3)</sup>	AD17	32
	33	FRAME#	GND	34
	35	GND	IRDY#	36
	37	DEVSEL#	+5V	38
	39	GND	LOCK#	40
	41	<i>Reserved</i>	<i>Reserved</i>	42
	43	PAR	GND	44
	45	VI/O <sup>3)</sup>	AD15	46
	47	AD12	AD11	48
	49	AD09	+5V	50
	51	GND	C/BE0#	52
	53	AD06	AD05	54
	55	AD04	GND	56
	57	VI/O <sup>3)</sup>	AD03	58
	59	AD02	AD01	60
	61	AD00	+5V	62
	63	GND	REQ64# <sup>2)</sup>	64

*pin positions printed italic/gray: reserved by specification / not connected*

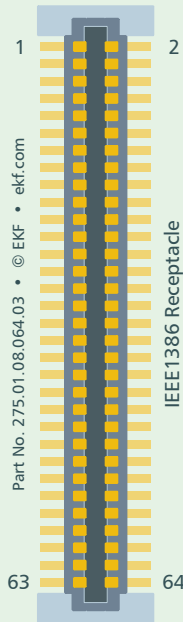
- 1) BUSMODE1# is an output signal by the PMC module (indicates that a suitable module is present). It is wired for convenience to GPIO1 of the PEX8112 PCIe to PCI bridge.
- 2) REQ64# and ACK64# (PMC-J12) are wired to pull-up resistors, indicating 32-bit PCI.
- 3) By default, VI/O is tied to +3.3V. As a stuffing option, the CCK-MARIMBA can be delivered with +5V VI/O.
- 4) -12V is not provided by the CPU carrier board. If -12V is actually required by a PMC module, it must be supplied externally, across the rear I/O connector J1.

PMC-J12 - PCI				
	1	+12V	TRST# <sup>4)</sup>	2
	3	TMS	TDO	4
	5	TDI	GND	6
	7	GND	Reserved	8
	9	Reserved	Reserved	10
	11	BUSMODE2# <sup>3)</sup>	+3.3V	12
	13	RST#	BUSMODE3# <sup>3)</sup>	14
	15	+3.3V	BUSMODE4# <sup>3)</sup>	16
	17	PME#	GND	18
	19	AD30	AD29	20
	21	GND	AD26	22
	23	AD24	+3.3V	24
	25	IDSEL <sup>1)</sup>	AD23	26
	27	+3.3V	AD20	28
	29	AD18	GND	30
	31	AD16	C/BE2#	32
	33	GND	Reserved	34
	35	TRDY#	+3.3V	36
	37	GND	STOP#	38
	39	PERR#	GND	40
	41	+3.3V	SERR#	42
	43	C/BE1#	GND	44
	45	AD14	AD13	46
	47	M66EN	AD10	48
	49	AD08	+3.3V	50
	51	AD07	Reserved	52
	53	+3.3V	Reserved	54
	55	Reserved	GND	56
	57	Reserved	Reserved	58
	59	GND	Reserved	60
	61	ACK64# <sup>2)</sup>	+3.3V	62
	63	GND	Reserved	64

*pin positions printed italic/gray: reserved by specification / not connected*

- 1) IDSEL is assigned to AD16
- 2) REQ64# (PMC-J11) and ACK64# are wired to pull-up resistors, indicating 32-bit PCI.
- 3) BUSMODE2# is tied to VI/O, and BUSMODE3# BUSMODE4# are tied to GND, indicating PCI protocol usage to PMC module
- 4) There is no JTAG I/F provided on the CCK-MARIMBA. However, TRST# has a pull-down resistor in order to avoid accidental enabling of the JTAG circuitry on a PMC module.

PMC-J14 - PCI				
1	PMC RIO 1	PMC RIO 2	2	
3	PMC RIO 3	PMC RIO 4	4	
5	PMC RIO 5	PMC RIO 6	6	
7	PMC RIO 7	PMC RIO 8	8	
9	PMC RIO 9	PMC RIO 10	10	
11	PMC RIO 11	PMC RIO 12	12	
13	PMC RIO 13	PMC RIO 14	14	
15	PMC RIO 15	PMC RIO 16	16	
17	PMC RIO 17	PMC RIO 18	18	
19	PMC RIO 19	PMC RIO 20	20	
21	PMC RIO 21	PMC RIO 22	22	
23	PMC RIO 23	PMC RIO 24	24	
25	PMC RIO 25	PMC RIO 26	26	
27	PMC RIO 27	PMC RIO 28	28	
29	PMC RIO 29	PMC RIO 30	30	
31	PMC RIO 31	PMC RIO 32	32	
33	PMC RIO 33	PMC RIO 34	34	
35	PMC RIO 35	PMC RIO 36	36	
37	PMC RIO 37	PMC RIO 38	38	
39	PMC RIO 39	PMC RIO 40	40	
41	PMC RIO 41	PMC RIO 42	42	
43	PMC RIO 43	PMC RIO 44	44	
45	PMC RIO 45	PMC RIO 46	46	
47	PMC RIO 47	PMC RIO 48	48	
49	PMC RIO 49	PMC RIO 50	50	
51	PMC RIO 51	PMC RIO 52	52	
53	PMC RIO 53	PMC RIO 54	54	
55	PMC RIO 55	PMC RIO 56	56	
57	PMC RIO 57	PMC RIO 58	58	
59	PMC RIO 59	PMC RIO 60	60	
61	PMC RIO 61	PMC RIO 62	62	
63	PMC RIO 63	PMC RIO 64	64	



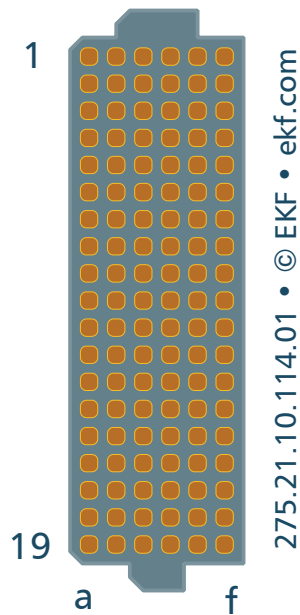
See table J1 for assignment of the PMC-J14 rear I/O signals to the rear I/O hard metric connector J1. Please contact sales@ekf.de for designing a custom specific rear I/O transition module. In addition, if high speed differential signals are required to be handed over from PMC-J14 to J1, a custom specific variant of the CCK-MARIMBA should be considered, in order to match impedance and trace length constraints of particular signal pairs.



### XMC Socket Receptacles J15 J16

ANSI/VITA 42.3 defines a primary XMC connector, which is mandatory (for PCIe fabric), and a secondary XMC connector, which is optional (either fabric or user I/O).

The CCK-MARIMBA is a XMC carrier board with a 4-Lane PCI Express host interface (primary connector XMC-J15). In addition, XMC-J16 is reserved for optional rear I/O usage across the connector J1 (custom specific rear I/O transition module).



XMC.3 Receptacle

Since the CPU carrier board provides a 4-lane PCI Express interface across the P-PCIE connector and there are further PCIe devices on the CCK-MARIMBA side board, a PCIe packet switch is used, with a primary PCIe port (1 link x 4 lanes), a secondary PCIe port (4 lanes) towards the XMC receptacle, and a third PCIe port for the on-board PCI bridge (PMC connectors) and on-board SATA controller. The total PCIe bandwidth therefore is shared between active PCI Express devices. Theoretically, a very high load on the SATA controller could slightly degrade the performance of a XMC Module organized as PCIe x 4, and vice versa.

Some PCIe packet switch GPIOs are used to detect XMC Module status information, or to emulate an I2C channel to the module, for convenience.

XMC Connector J15 - PCIe Fabric • EKF Part No. 275.21.10.114.01						
	a	b	c	d	e	f
1	PETOP0	PETON0	+3.3V	PETOP1	PETON1	+5V
2	GND	GND	TRST# <sup>1)</sup>	GND	GND	MRSTI# <sup>6)</sup>
3	PETOP2	PETON2	+3.3V	PETOP3	PETON3	+5V
4	GND	GND	TCK	GND	GND	MRSTO# <sup>7)</sup>
5	<i>PETOP4</i>	<i>PETON4</i>	+3.3V	<i>PETOP5</i>	<i>PETON5</i>	+5V
6	GND	GND	TMS	GND	GND	+12V
7	<i>PETOP6</i>	<i>PETON6</i>	+3.3V	<i>PETOP7</i>	<i>PETON7</i>	+5V
8	GND	GND	TDI	GND	GND	-12V <sup>8)</sup>
9	<i>RFU</i>	<i>RFU</i>	<i>RFU</i>	<i>RFU</i>	<i>RFU</i>	+5V
10	GND	GND	TDO	GND	GND	GA0 <sup>3)</sup>
11	PEROP0	PERON0	MBIST# <sup>2)</sup>	PEROP1	PERON1	+5V
12	GND	GND	GA1 <sup>3)</sup>	GND	GND	MPRESENT# <sup>9)</sup>
13	PEROP2	PERON2	+3.3V <sup>4)</sup>	PEROP3	PERON3	+5V
14	GND	GND	GA2 <sup>3)</sup>	GND	GND	MSDA <sup>10)</sup>
15	<i>PEROP4</i>	<i>PERON4</i>	<i>RFU</i>	<i>PEROP5</i>	<i>PERON5</i>	+5V
16	GND	GND	MVMRO <sup>5)</sup>	GND	GND	MSCL <sup>10)</sup>
17	<i>PEROP6</i>	<i>PERON6</i>	<i>RFU</i>	<i>PEROP7</i>	<i>PERON7</i>	<i>RFU</i>
18	GND	GND	<i>RFU</i>	GND	GND	<i>RFU</i>
19	CLKP_XMC	CLKN_XMC	<i>RFU</i>	WAKE#	ROOT0#	<i>RFU</i>

*pin positions printed italic/gray: reserved by specification / not connected*

- <sup>1)</sup> TRST# has a 1k PD in order to avoid inadvertent activation of the JTAG port
- <sup>2)</sup> MBIST# (Module Built In Self Test) is an optional output by the XMC module, connected to PCI Express switch PES12T3 GPIO04
- <sup>3)</sup> GA0 GA1 GA2 (I2C address assigned to module) tied to GND
- <sup>4)</sup> Module +3.3V AUX
- <sup>5)</sup> MVMRO (Module Volatile Memory Read Only) is an optional input to the XMC module, connected to PCI Express switch PES12T3 GPIO11 (1k PD resistor, write enable by default)
- <sup>6)</sup> MRSTI# (Module Reset Input) tied to platform reset
- <sup>7)</sup> MRSTO# (Module Reset Output) is an optional output by the XMC module, connected to PCI Express switch PES12T3 GPIO02
- <sup>8)</sup> -12V is not provided by the CPU carrier board. If -12V is actually required by a XMC module, it must be supplied externally, across the rear I/O connector J1
- <sup>9)</sup> MPRESENT# (Module Present), connected to PCI Express switch PES12T3 GPIO03
- <sup>10)</sup> MSCL/MSDA (Module Serial Clock/Data), connected to PCI Express switch PES12T3 GPIO05/06 which have to be configured as I2C master controller port for potential usage of I2C slave devices on the XMC module

## XMC Connector J16 - User I/O • EKF Part No. 275.21.10.114.01

	a	b	c	d	e	f
1			XMC RIO C01			XMC RIO F01
2	GND	GND	XMC RIO C02	GND	GND	XMC RIO F02
3			XMC RIO C03			XMC RIO F03
4	GND	GND	XMC RIO C04	GND	GND	XMC RIO F04
5			XMC RIO C05			XMC RIO F05
6	GND	GND	XMC RIO C06	GND	GND	XMC RIO F06
7			XMC RIO C07			XMC RIO F07
8	GND	GND	XMC RIO C08	GND	GND	XMC RIO F08
9			XMC RIO C09			XMC RIO F09
10	GND	GND	XMC RIO C10	GND	GND	XMC RIO F10
11			XMC RIO C11			XMC RIO F11
12	GND	GND	XMC RIO C12	GND	GND	XMC RIO F12
13			XMC RIO C13			XMC RIO F13
14	GND	GND	XMC RIO C14	GND	GND	XMC RIO F14
15			XMC RIO C15			XMC RIO F15
16	GND	GND	XMC RIO C16	GND	GND	XMC RIO F16
17			XMC RIO C17			XMC RIO F17
18	GND	GND	XMC RIO C18	GND	GND	XMC RIO F18
19			XMC RIO C19			XMC RIO F19

*empty pin positions: not connected*

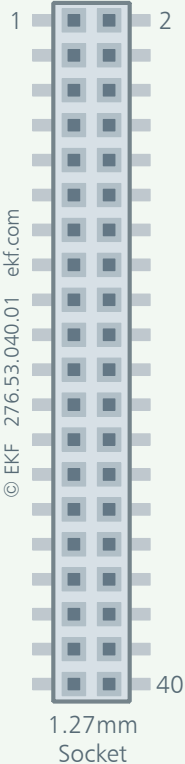
See table J1 for assignment of the XMC-J16 rear I/O signals to the rear I/O hard metric connector J1. Please contact [sales@ekf.de](mailto:sales@ekf.de) for designing a custom specific rear I/O transition module. In addition, if high speed differential signals are required to be handed over from XMC-J16 to J1, a custom specific variant of the CCK-MARIMBA should be considered, in order to match impedance and trace length constraints of particular signal pairs.

## P-IDE2

The CCK-MARIMBA is provided with the JMB363 PCIe to SATA/PATA bridge. The PATA (IDE) signals are routed to the optional socket P-IDE2.

P-IDE2, if populated, is a bottom mount connector, suitable for a bottom mount CompactFlash mezzanine module (C17-CFA).

### P-IDE2 CompactFlash/IDE Expansion Interface 1.27mm Socket 2 x 20 (276.53.040.01)

 <p>© EKF 276.53.040.01 ekf.com</p> <p>1.27mm Socket</p> <p>top view pin numbering order (P-IDE1)</p>	IDE0_RESET#	1	2	GND
	IDE0_DD07	3	4	IDE0_DD08
	IDE0_DD06	5	6	IDE0_DD09
	IDE0_DD05	7	8	IDE0_DD10
	IDE0_DD04	9	10	IDE0_DD11
	IDE0_DD03	11	12	IDE0_DD12
	IDE0_DD02	13	14	IDE0_DD13
	IDE0_DD01	15	16	IDE0_DD14
	IDE0_DD00	17	18	IDE0_DD15
	GND	19	20	+3.3V_CR *
	IDE0_DMARQ	21	22	+3.3V_CR *
	IDE0_DIOW#	23	24	GND
	IDE0_DIOR#	25	26	GND
	IDE0_IORDY	27	28	+5V_CR *
	IDE0_DMACK#	29	30	+5V_CR *
	IDE0_INTRQ	31	32	GND
	IDE0_DA1	33	34	IDE_CBLID#
	IDE0_DAO	35	36	IDE0_DA2
	IDE0_CS0#	37	38	IDE0_CS1#
	IDE0_ACT#	39	40	GND

\* switched power supply lines from CPU carrier board according to Sx state

## P-SATA1

The CCK-MARIMBA is equipped with the JMB363 PCIe to single port PATA, dual port SATA controller (i.e. up to 4 mass storage devices in total). It provides two Serial ATA II channels, which are routed to the optional on-board connector P-SATA1. This is a high speed signal connector, suitable for attachment of the C20-SATA mezzanine module.

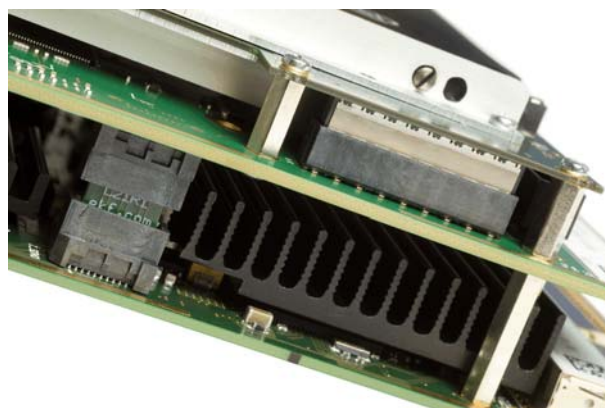
The C20-SATA is an optional storage module, which can be equipped with up to two 2.5-inch SATA drives, mounted back to back (one on top, one on bottom of the C20-SATA PCB).



C20-SATA (Single Drive)

Typically, SATA drives require +5V as power source. The CCK-MARIMBA takes this voltage either from the carrier CPU board (+5V\_CR), which is a switched power line according to the S-state of the CPU, or as an alternative from the CCK-MARIMBA rear I/O connector J1. Selection is done by CCK-MARIMBA stuffing option, by means of a Polyswitch resettable 1.5A fuse populated on either one of the power lines. By default, +3.3V and +12V are not passed from the CCK-MARIMBA to the C20-SATA mezzanine module - contact EKF if this is a requirement (available as stuffing option).

The JMB363 is a very popular SATA controller, which allows for several operating modes, including RAID 0, 1, 0+1. Drivers can be downloaded for Windows (WHQL certified) or Linux from <ftp://driver.jmicron.com.tw>.





C20-SATA

P-SATA1 is available as a stuffing option. There is another SATA I/O variant available, via P-SATA2 and P-SATA3 (7-position headers for attachment of latched SATA cables). Both options are provided only exclusive to each other - please select before ordering the CCK-MARIMBA.

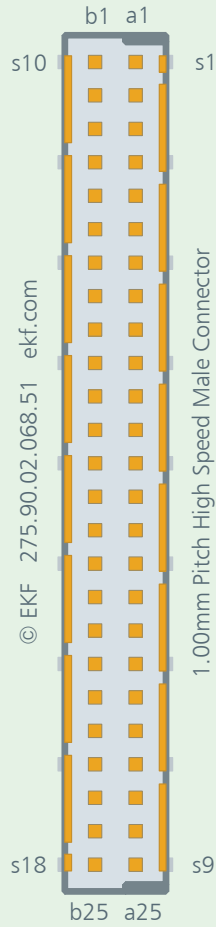


C20-SATA Top View



C20-SATA Bottom View (Dual Drive)

P-SATA1 SATA Expansion Interface  
1.00mm Pitch Male Connector 2mm Height (275.90.02.068.51)



GND	b1	a1	GND
	b2	a2	SATA0_TXP
	b3	a3	SATA0_TXN
GND	b4	a4	GND
	b5	a5	SATA0_RXN
	b6	a6	SATA0_RXP
GND	b7	a7	GND
	b8	a8	SATA1_TXP
	b9	a9	SATA1_TXN
GND	b10	a10	GND
	b11	a11	SATA1_RXN
	b12	a12	SATA1_RXP
GND	b13	a13	GND
	b14	a14	
	b15	a15	
GND	b16	a16	GND
	b17	a17	
	b18	a18	
	b19	a19	
	b20	a20	
	b21	a21	
+5V_SATA	b22	a22	+3.3V_SATA
+5V_SATA	b23	a23	+3.3V_SATA
	b24	a24	
	b25	a25	

Notes:

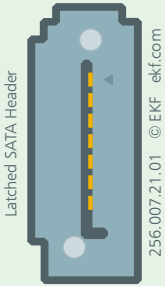
- ▶ +3.3V\_SATA is not connected by default - can be tied to either +3.3V\_CR or +3.3V\_EXT as stuffing option
- ▶ +5V\_SATA by default is connected to +5V\_CR across 1.5A PolySwitch resettable fuse - can be tied to +5V\_EXT as stuffing option
- ▶ All sx pins (shield) are tied to GND
- ▶ All TX/RX designations with respect to SATA controller (TX controller = RX drive, RX controller = TX drive)



### P-SATA2 P-SATA3

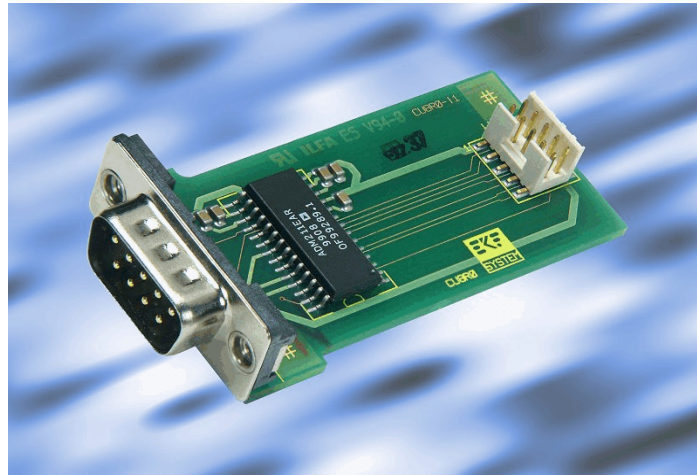
The CCK-MARIMBA can be optionally stuffed with two vertical latched SATA signal headers. TX/RX designation of signals is with respect to the SATA controller. P-SATA2 corresponds to the SATA channel 0 of the JMB363 controller, and P-SATA3 is wired to the JMB363 SATA channel 1.

Usage of P-SATA2/3 is available only exclusive to P-SATA1 - discuss your actual needs with sales@ekf.de before ordering. Mixed stuffing of P-SATA1 (single channel SATA operation) and either one of P-SATA2 or P-SATA3 is also an option.

P-SATA2	P-SATA3	#256.007.21.01	Latched Headers	
			1	GND
			2	SATA_TX+
			3	SATA_TX-
			4	GND
			5	SATA_RX-
			6	SATA_RX+
			7	GND

## P-SP3 P-SP4

The on-board SIO (Super I/O controller) provides up to four serial interfaces (UART, DOS COM ports). While the serial ports SP1 und SP2 are wired to the optional rear I/O connector J2 only, another two UARTs are available in addition from the optional pin headers P-SP3 and P-SP4 (TTL-level on all signals). P-SP3 and P-SP4 are suitable for attachment of EKF CU-series PHY modules via a micro ribbon flat cable assembly. A PHY module is a transceiver from TTL level signals to a specific symmetric or asymmetric interface standard, e.g. EIA-485 or RS-232E, with or w/o galvanic isolation. Please contact [sales@ekf.de](mailto:sales@ekf.de) for availability of different CU-series modules (inquiries for custom specific PHY or transition modules welcome). Also custom specific front panel design can be done.



CU-Series PHY Module

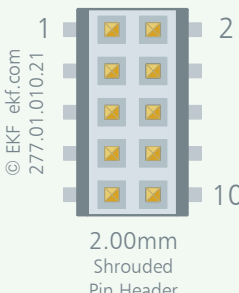
Due to another (primary) SIO typically available on the CCG-RUMBA host board, the serial interfaces are not necessarily assigned to COM-1/COM-4 by the operating system. Verify or modify the accompanying CCG-RUMBA BIOS settings for mapping of physical asynchronous serial I/O ports to the logical COM port order.

Alternatively the connectors P-SP3 and/or P-SP4 can be used as 5V tolerant programmable I/O (GPIO). Details can be derived from the SCH3114 Super I/O controller data sheet ([www.smsc.com](http://www.smsc.com)).

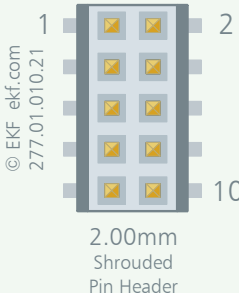
In addition, the serial ports 3 and 4 are also available for rear I/O across J2 (option). In order to avoid signal interference, attach a transceiver module or other circuitry either on-board to P-SP3/4, or on the rear I/O transition module, but not both.

A special signal pair may be used as GPO for alternate purposes (not in use by default):

- ▶ SP4\_DTR# can be configured (stuffing option) as SMBus EEPROM address line A1
- ▶ SP4\_RTS# can be configured as SMBus EEPROM Write Protect WP

P-SP3 TTL-Level Serial I/O or GPIO 2.00mm Pin Header 2 x 5 (277.01.010.21)				
	+5V_SP3 0.5A <sup>1</sup>	1	2	DSR3# / GP12
	RI3# / GP13	3	4	RXD3 / GP10
	TXD3 / GP11	5	6	DTR3# / GP15
	RTS3# / GP17	7	8	CTS3# / GP16
	DCD3# / GP12	9	10	GND

<sup>1</sup> short circuit protection by a PolySwitch resettable fuse, voltage derived from +5V\_CR carrier board switched power well

P-SP4 TTL-Level Serial I/O or GPIO 2.00mm Pin Header 2 x 5 (277.01.010.21)				
	+5V_SP4 0.5A <sup>1</sup>	1	2	DSR4# / GP66
	RI4# / GP31	3	4	RXD4 / GP64
	TXD4 / GP65	5	6	DTR4# / GP34 **
	RTS4# / GP67 **	7	8	CTS4# / GP62
	DCD4# / GP63	9	10	GND

<sup>1</sup> short circuit protection by a PolySwitch resettable fuse, voltage derived from +5V\_CR carrier board switched power well

\*\* SMBus EEPROM A1 can be optionally controlled (stuffing option) by SIO GP34 (serial port 4 DTR#), SMBus EEPROM WP is likewise tied to GP67 (serial port 4 RTS4#)

P-UFD2

As an option, the CCK-MARIMBA can be equipped with a connector for an industrial style USB Flash disk mezzanine module. The connector is a 2.0mm pitch pin header, suitable for a low profile SSD (Solid-State Drive) 37mm x 26mm. As of current, such modules are available e.g. from STEC, Intel, SanDisk and other manufacturers, up to 8GByte.

P-UFD ○ 2.00mm Pin Header 2x5 (251.1.0205.20.01) USB Solid-State Drive (Low Profile) 562.20.0004.00 (4GB) STec SLUFDM • Intel Z-U130 SSDUSMS • SanDisk SDUS5EB				
	+5V_CR	1	2	NC
	USB+	3	4	NC
	USB-	5	6	NC
	GND	7	8	NC
	Mech. Key	9	10	NC



USB SSD

The P-UFD2 USB data signals are derived from the USB root hub (ICH southbridge) on the CPU carrier board via P-EXP. There are two USB channels available on the CCK-MARIMBA, both wired by default for rear I/O across the optional connector J2. With P-UFD2 filled however, one USB port is assigned to P-UFD2, and therefore not available for rear I/O.

The connector P-UFD2 is located on bottom of the CCK-MARIMBA, and is available as a stuffing option. Please specify your need for P-UFD2 before ordering.



## On-Board Jumpers

Most options on the CCK-MARIMBA are stuffing options, so there are only 2 jumpers which are available for user interaction, J-RES (force reset) and J-FWH2 (select Firmware Hub).

### J-RES Reset

Provided as an option, the pin header J-RES can be used for resetting the CPU host board (processor reset) if wired to additional circuitry (e.g. watchdog or manual pushbutton). Tie reset# to GND with an open collector output. While debugging the system, a 2.54mm jumper may be used to force a manual reset.

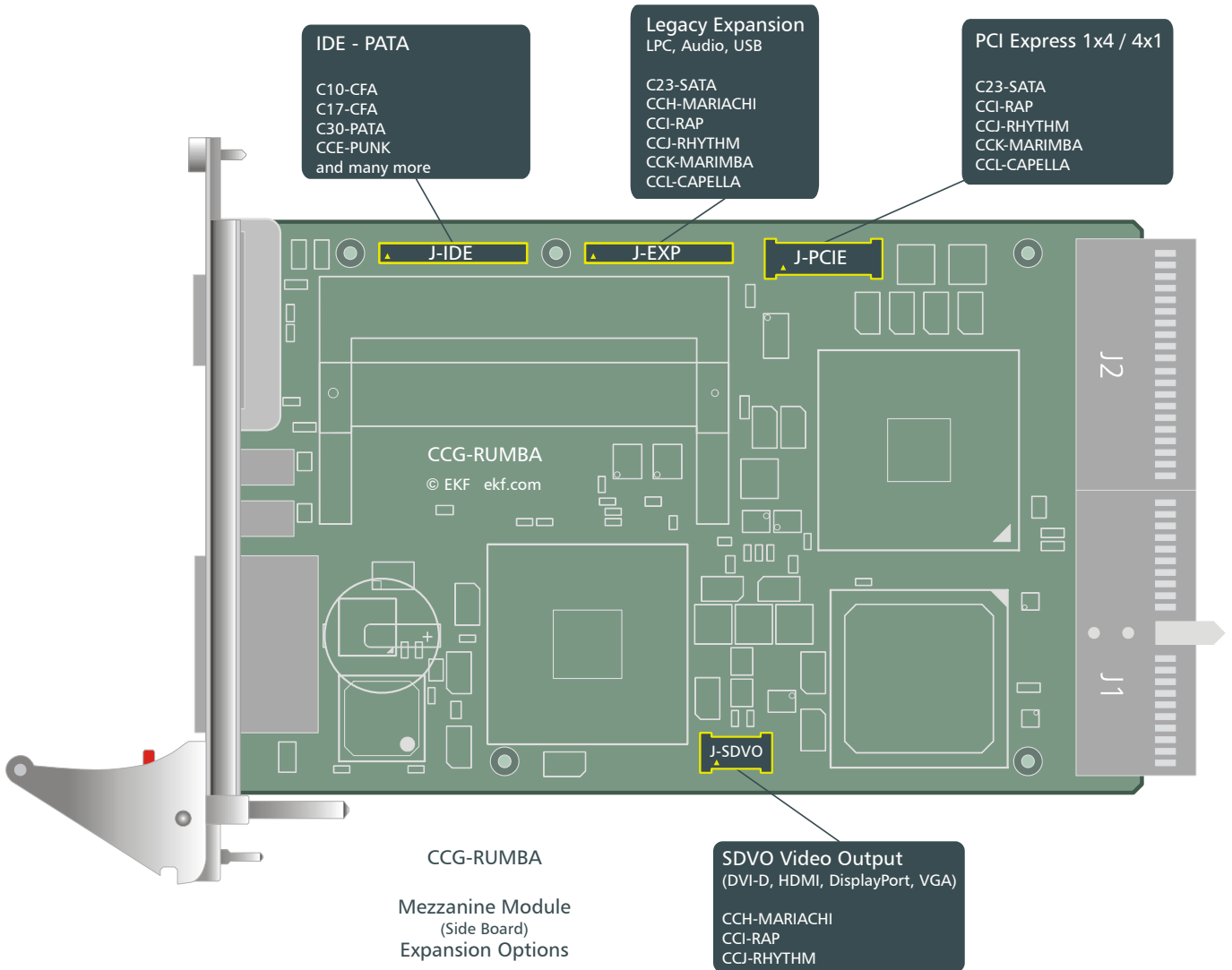


### J-FWH2

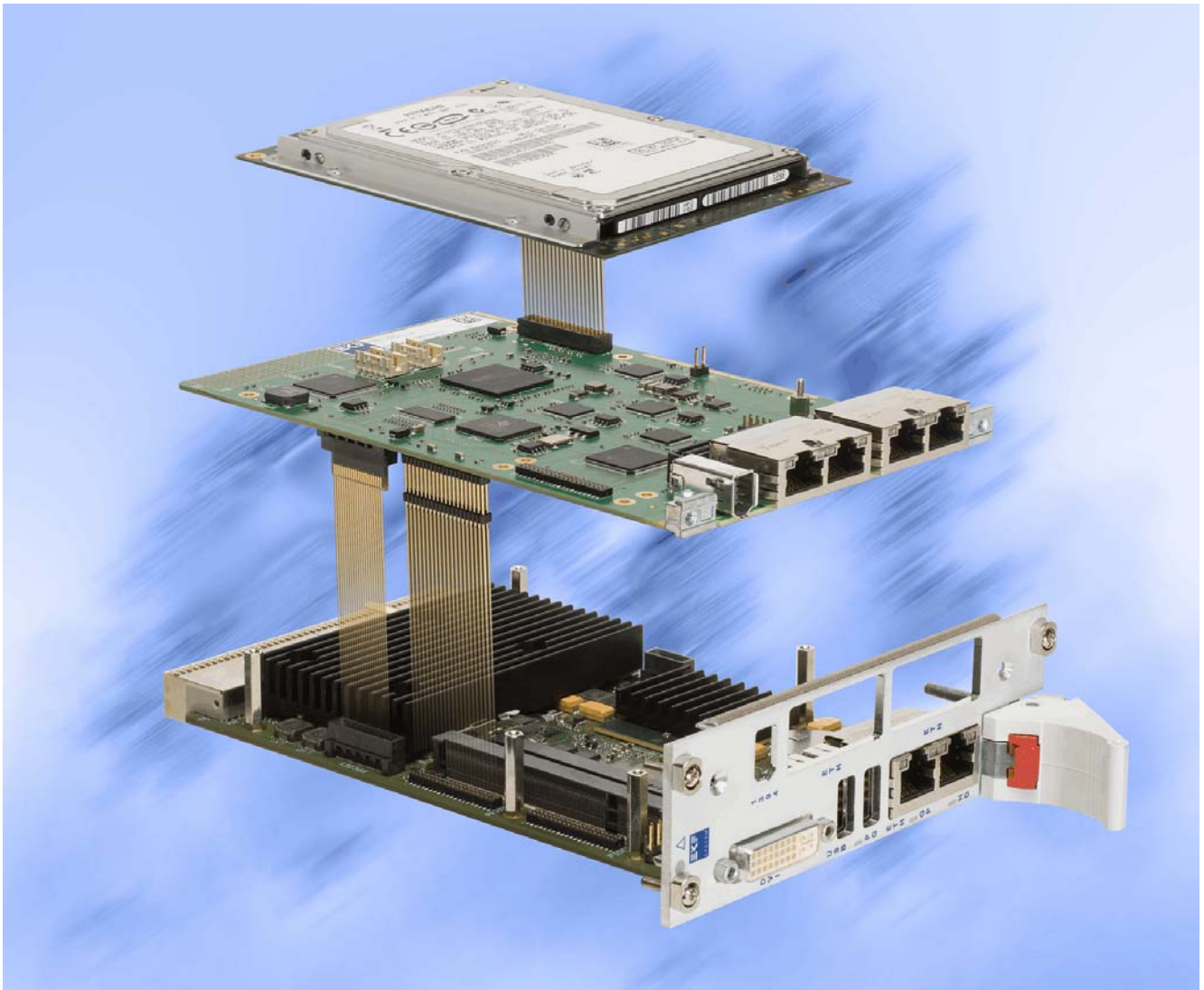
Please see description in chapter 'Firmware Hub 2'.

## Inter-Board Connectors

The CCK-MARIMBA side board is equipped with 2 inter-board connectors, which are related to the CPU carrier board host. These are the P-EXP (LPC and mixed signals), and the P-PCIe (4-Lane PCI Express) connectors. All inter-board connectors are situated at the bottom of the CCK-MARIMBA and establish the data path and power link to the carrier board CPU. As the CCK-MARIMBA comes typically mounted as a unit together with the CCG-RUMBA, there is normally no need for the user to get access to any of the inter-board connectors. They are described here as a reference only and for better understanding of the CCK-MARIMBA.

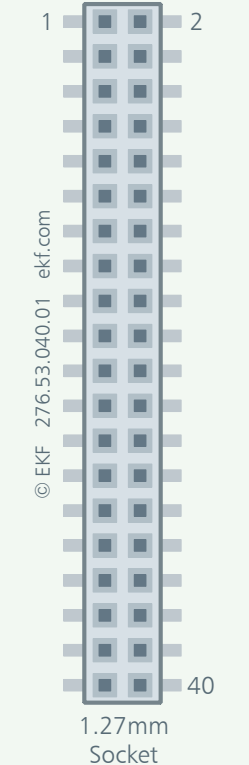


The picture below illustrates a typical mezzanine stack, comprised of the CPU carrier board (shared front panel from 4HP to 12HP, individually tailored to customers configuration), the mezzanine side board (shown here CCL-CAPELLA), and a SATA storage module (either SSD or hard disk, 1.8-inch or 2.5-inch, dual or single drive, RAID option).



## P-EXP

The inter-board connector P-EXP is mounted on bottom of the CCK-MARIMBA PCB, with its face aligned towards the corresponding connector on the CCG-RUMBA. This allows to attach the CCK-MARIMBA mezzanine companion card on top of the CPU carrier board. A suitable board stacker is used in addition to bridge the gap between the two boards (exactly 4HP distance between PCBs). P-EXP is used to pass the Low Pin Count I/F to the CCK-MARIMBA, besides USB channels and other sideband signals.

P-EXP Expansion Board Interface (LPC/HDAudio/USB) 1.27mm Socket 2 x 20 (276.53.040.01)				
 <p>pin orientation shows CPU carrier board top view</p>	GND	1	2	+3.3V_CR *
	CLK_33MHZ	3	4	PLTRST#
	LPC_AD0	5	6	LPC_AD1
	LPC_AD2	7	8	LPC_AD3
	LPC_FRAME#	9	10	LPC_DRQ#
	GND	11	12	+3.3V_CR *
	SERIRQ	13	14	PME#
	SMI#	15	16	CLK_14MHZ
	FWH_ID0	17	18	FWH_INIT#
	KBD_RST#	19	20	A20GATE
	GND	21	22	+5V_CR *
	USB_P2N <sup>1</sup>	23	24	USB_P1N <sup>2</sup>
	USB_P2P <sup>1</sup>	25	26	USB_P1P <sup>2</sup>
	USB_OC# <sup>3</sup>	27	28	DBRESET#
	SMB_CLK	29	30	SMB_DAT
	GND	31	32	+5V_CR *
	PE Port Cfg Bit 1 <sup>4</sup> <i>HDA_SDOOUT</i>	33	34	<i>HDA_SDINO</i>
	<i>HDA_RST#</i>	35	36	PE Port Cfg Bit 0 <sup>4</sup> <i>HDA_SYNC</i>
	<i>HDA_BITCLK</i>	37	38	<i>HDA_SDIN1</i>
	SPEAKER	39	40	+12V_CR

<sup>1</sup> connects to USB Port 6 on CCG-RUMBA

<sup>2</sup> connects to USB Port 5 on CCG-RUMBA

<sup>3</sup> connects to USB\_OC56# on CCG-RUMBA

<sup>4</sup> PCI Express port configuration is strapped to 1 link x 4 lanes on the CCK-MARIMBA

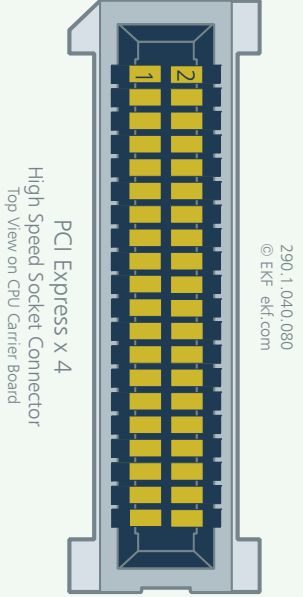
\* switched power supply lines from CPU carrier board according to Sx state



## P-PCIE

The high speed expansion socket P-PCIE is mounted on bottom of the CCK-MARIMBA. This allows to attach the mezzanine companion card on top of the CPU carrier board. A mating strip line PCB (C22-PCIEX2) is used in addition to bridge the gap between the two boards, which results from the horizontal 0.8-inch (20.32mm) card slot pitch.

P-PCIE is organized as a 1x4 link (4 aggregated PCIe lanes form a link) on the CCK-MARIMBA (refer to hardware strapping signals on P-EXP which indicate the link status to the ICH southbridge on the CPU carrier card).

P-PCIE PCI Express x 4 High Speed Dual Row Socket 0.8mm Pitch 290.1.040.080				
 <p>pin orientation shows CPU carrier board top view (see-trough CCK-MARIMBA PCB)</p>	GND	1	2	GND
	+5V_CR <sup>1</sup>	3	4	+3.3V_CR <sup>1</sup>
	+5V_CR <sup>1</sup>	5	6	+3.3V_CR <sup>1</sup>
	GND	7	8	GND
	PE_CLKP	9	10	PE_RST#
	PE_CLKN	11	12	PE_WAKE#
	GND	13	14	GND
	PE0_TP	15	16	PE0_RP
	PE0_TN	17	18	PE0_RN
	GND	19	20	GND
	GND	21	22	GND
	PE1_TP	23	24	PE1_RP
	PE1_TN	25	26	PE1_RN
	GND	27	28	GND
	PE2_TP	29	30	PE2_RP
	PE2_TN	31	32	PE2_RN
	GND	33	34	GND
	PE3_TP	35	36	PE3_RP
	PE3_TN	37	38	PE3_RN
	GND	39	40	+12V_CR

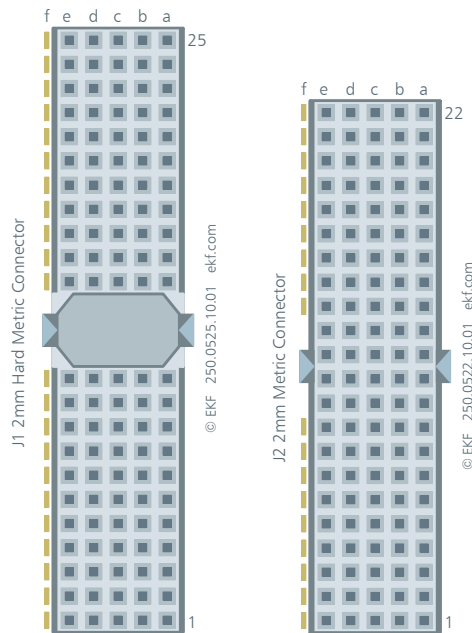
<sup>1</sup> switched on/off power lines on CCG-RUMBA CPU carrier board according to S3 state

## Rear I/O Connectors

### J1 J2

As an option, the CCK-MARIMBA can be equipped with the rear I/O connectors J1 and J2. A single slot rear I/O backplane (directly adjoining the CPCI backplane) would be required for handing over the available signal lines to a suitable rear I/O transition module.

The CCK-MARIMBA must not be plugged into a common CPCI slot in order to avoid damaging the board or other components of the system. A brown key on the J1 connector will prevent the user from erroneously inserting the CCK-MARIMBA into an unsuitable position.



Signal names provided on the J1 and J2 connector tables hereafter are associated with their main function. However, the Super I/O controller allows a number of signals also be used as general purpose I/O. Please consult the SMSC SCH3114 datasheet for details ([www.smsc.com](http://www.smsc.com)).

Please note, that the majority of signals is also available on-board or via front panel. Be sure to have connected any signal only once, in order to avoid interference.

#J1	A	B	C	D	E
25	PMC_J14_01	PMC_J14_02	GND	PMC_J14_03	PMC_J14_04
24	PMC_J14_05	PMC_J14_06	PMC_J14_07	PMC_J14_08	PMC_J14_09
23	PMC_J14_10	PMC_J14_11	PMC_J14_12	PMC_J14_13	PMC_J14_14
22	PMC_J14_15	PMC_J14_16	PMC_J14_17	PMC_J14_18	PMC_J14_19
21	PMC_J14_20	PMC_J14_21	PMC_J14_22	PMC_J14_23	PMC_J14_24
20	PMC_J14_25	PMC_J14_26	PMC_J14_27	PMC_J14_28	PMC_J14_29
19	PMC_J14_30	PMC_J14_31	PMC_J14_32	PMC_J14_33	PMC_J14_34
18	PMC_J14_35	PMC_J14_36	PMC_J14_37	PMC_J14_38	PMC_J14_39
17	PMC_J14_40	PMC_J14_41	PMC_J14_42	PMC_J14_43	PMC_J14_44
16	PMC_J14_45	PMC_J14_46	PMC_J14_47	PMC_J14_48	PMC_J14_49
15	PMC_J14_50	PMC_J14_51	PMC_J14_52	PMC_J14_53	PMC_J14_54
14	KEY (BROWN)				
13					
12					
11	PMC_J14_55	PMC_J14_56	PMC_J14_57	PMC_J14_58	PMC_J14_59
10	PMC_J14_60	PMC_J14_61	PMC_J14_62	PMC_J14_63	PMC_J14_64
9	+5V_EXT *	+3.3V_EXT *	GND	-12V_EXT *	+12V_EXT *
8	XMC_J16_C01	XMC_J16_C02	GND	XMC_J16_F01	XMC_J16_F02
7	XMC_J16_C03	XMC_J16_C04	XMC_J16_F03	XMC_J16_F04	XMC_J16_F05
6	XMC_J16_C05	XMC_J16_C06	XMC_J16_C07	XMC_J16_F06	XMC_J16_F07
5	XMC_J16_C08	XMC_J16_C09	XMC_J16_F08	XMC_J16_F09	XMC_J16_F10
4	XMC_J16_C10	XMC_J16_C11	XMC_J16_C12	XMC_J16_F11	XMC_J16_F12
3	XMC_J16_C13	XMC_J16_C14	XMC_J16_F13	XMC_J16_F14	XMC_J16_F15
2	XMC_J16_C15	XMC_J16_C16	XMC_J16_C17	XMC_J16_F16	XMC_J16_F17
1	XMC_J16_C18	XMC_J16_C19	GND	XMC_J16_F18	XMC_J16_F19

\* optional external supply voltages for PMC/XMC, +5V\_EXT optionally in use as disk drive power source

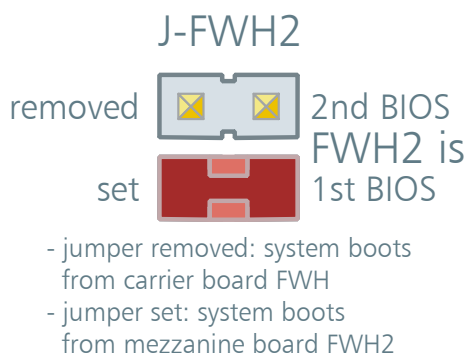
#J2	A	B	C	D	E
22	+5V_CR	+3.3V_CR	RSVD	RSVD	+12V_CR
21	GND	GND	GND	GND	GND
20	SP1_RI#	SP1_CTS#	SP2_RI# / GP50	SP2_CTS# / GP56	RSVD
19	SP1_RXD	GND	SP2_RXD / GP52	GND	FWH_GPI1
18	SP1_DSR#	SP1_DCD#	SP2_DSR# / GP54	SP2_DCD# / GP51	FWH_GPI2
17	SP1_DTR# 3)	GND	SP2_DTR# / GP57	GND	GND
16	SP1_RTS# 3)	SP1_TXD	SP2_RTS# / GP55 3)	SP2_TXD / GP53	DBRESET#
15	RSVD	GND	RSVD	GND	RSVD
14	SP3_RI# / GP13	SP3_CTS# / GP16	SP4_RI# / GP31	SP4_CTS# / GP62	SMB_DAT 1)
13	SP3_RXD / GP10	GND	SP4_RXD / GP64	GND	SMB_CLK 1)
12	SP3_DSR# / GP14	SP3_DCD# / GP12	SP4_DSR# / GP66	SP4_DCD# / GP63	GND
11	SP3_DTR# / GP15	GND	SP4_DTR# / GP34 2)	GND	USB1_D- 4)
10	SP3_RTS# / GP17	SP3_TXD / GP11	SP4_RTS# / GP67 2)	SP4_TXD / GP65	USB1_D+ 4)
9	RSVD	GND	RSVD	GND	GND
8	LPT_SLCT	LPT_PE	LPT_BUSY	SIO_GP47	USB_OC#
7	LPT_ACK#	GND	GND	SIO_GP46	GND
6	LPT_D7	LPT_D6	LPT_D5	SIO_GP45	USB2_D- 4)
5	LPT_D4	GND	LPT_D3	SIO_GP44	USB2_D+ 4)
4	LPT_D2	LPT_D1	LPT_SLCTIN#	SPEAKER	GND
3	LPT_D0	GND	LPT_INIT#	KBDAT	KBCLK
2	LPT_ALF#	LPT_ERROR#	LPT_STROBE#	GND	+5V_CR
1	GND	GND	GND	MSDAT	MSCLK

- 1) stuffing option: SM Bus signals buffered via LTC4300A-3, voltage level @ +5V\_CR  
buffer enable input is controlled by GP40 SCH3114 SIO (high=enabled)
- 2) GP34 may be used to control serial EEPROM A1 (stuffing option)  
GP67 may be used to control serial EEPROM WP (stuffing option)
- 3) These serial port handshake signals may be also in use for power up strapping options of the SCH3114 SIO (10k PU or PD) with no or minor impact on normal operation
- 4) Stuffing option - USB port(s) may be in use for on-board Solid State Disk(s)

## Additional Functions

### Firmware Hub 2

The CCK-MARIMBA is optionally provided with a 82802 compatible 8Mbit Flash (Firmware Hub), which can be used either as alternative boot BIOS, as an expansion memory to the CPU board BIOS, or for BIOS retrieval/rescue. The Firmware Hub is connected to the LPC (Low Pin Count) interface. The device ID of a particular FWH determines whether it is detected as BIOS after power on (ID = 0). If stuffed, the jumper J-FWH sets the on-board FWH2 ID to zero (and simultaneously changes the CCG-RUMBA SPI Flash BIOS ID to 1) - hence the system will use the BIOS on the CCK-MARIMBA after power-on.



A programming tool for the Firmware Hub and latest BIOS releases can be obtained from the EKF website.

### SMBus EEPROM

The CCK-MARIMBA is provided with a 24C01 1Kbit I<sup>2</sup>C EEPROM, for storing board configuration data. The EEPROM is accessed via the SMBus. If there is need for storing additional customer data, EKF can place an EEPROM instead with custom specific data space, e.g. 24C16.

If required, the SMBus EEPROM A1 can be optionally controlled (stuffing option) by SIO GP34 (serial port 4 DTR#), and the SMBus EEPROM WP is likewise tied to GP67 (serial port 4 RTS4#).

## Trusted Platform Module

The CCK-MARIMBA can be optionally equipped with a Trusted Platform Module cryptographic chip according to the TPM 1.2 specification. The board provides a footprint which is suitable for

- ▶ SLB9635 (Infineon [www.infineon.com/tpm](http://www.infineon.com/tpm))
- ▶ AT97SC3203 (Atmel [www.atmel.com](http://www.atmel.com))

and other brands. The TPM chip communicates with the CPU carrier board through the LPC interface. Recent operating systems such as Windows Vista and Linux provide TPM software support.

Typically, TPM chip manufacturers provide the necessary device driver software for integration into special operating systems, along with BIOS drivers. Full documentation for TCG primitives can be found in the TCG TPM Main Specification, Parts 1 – 3, on the TCG website located at <https://www.trustedcomputinggroup.org/>. TPM features specific to PC Client platforms are specified in the “TCG PC Client Specific TPM Interface Specification, Version 1.2”, also available on the TCG web site. Implementation guidance for 32-bit PC platforms is outlined in the “TCG PC Client Specific Implementation Specification for Conventional BIOS for TCG Version 1.2”, also available on the TCG web site.

Atmels TPM includes a cryptographic accelerator capable of computing a 2048-bit RSA signature in 500 ms and a 1024-bit RSA signature in 100ms. Performance of the SHA-1 accelerator is 50us per 64-byte block. TCG key generation operations will be completed using a proprietary mechanism in less than 1 msec. The TPM is offered to OEM manufacturers as a turnkey solution, including the firmware integrated on the chip.

Infineons security controllers have achieved the industry's highest rating for digital security, the Common Criteria EAL 5 high Certificate issued by the German government agency responsible for security in information technology. Infineon provides OEMs with a complete TCG solution that includes all required hardware, software, and management utilities to develop a complete platform security solution.

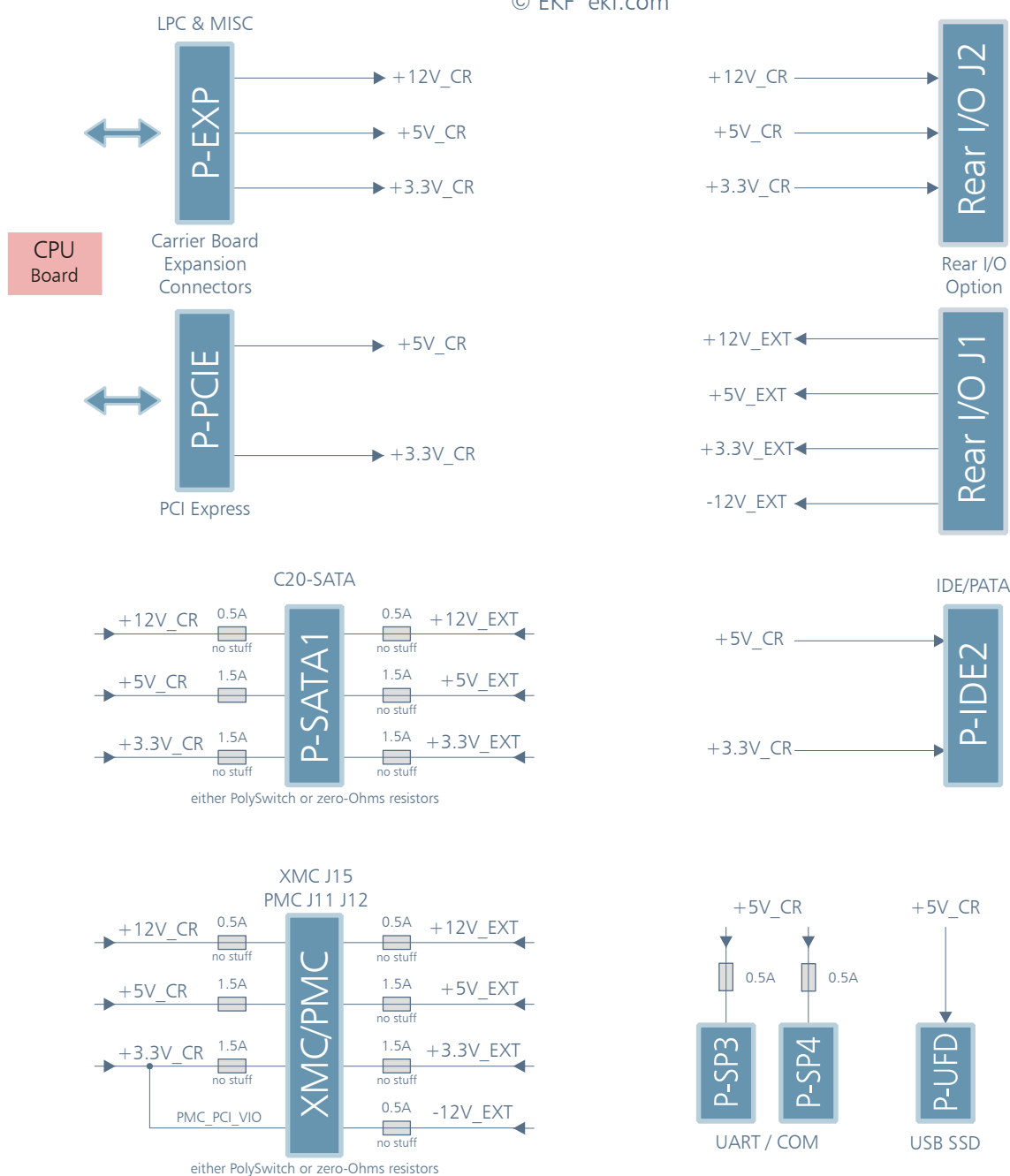
## Power Distribution

The CCK-MARIMBA gets its power from two sources: The CPU carrier board supplies +3.3V\_CR, +5V\_CR, and +12V\_CR, which may be switched off according to the current system sleep state. In addition, the rear I/O connector J1 can also be used to deliver alternate power to the SATA drives (+5V\_EXT, +3.3V\_EXT), and to the FireWire front panel connectors (+12V\_EXT).

For the C20-SATA hard disk drive mezzanine module, the +5V power source can be selected by a Polyswitch resettable fuse (stuffing option) between +5V\_CR and +5V\_EXT. The 1394 +12V bus power is derived concurrently from both, the carrier board +12V\_CR, and the J1 +12V\_EXT (back-driving protection by Schottky diodes).

### Power Distribution CCK-MARIMBA

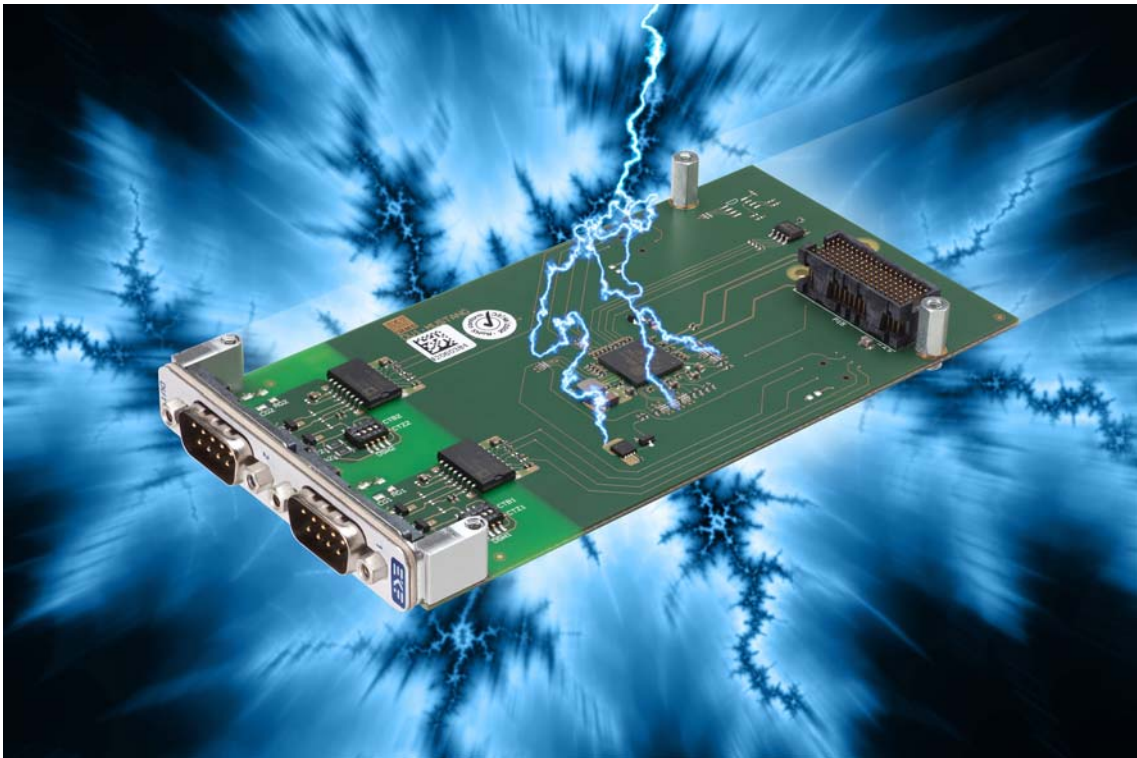
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## Schematics

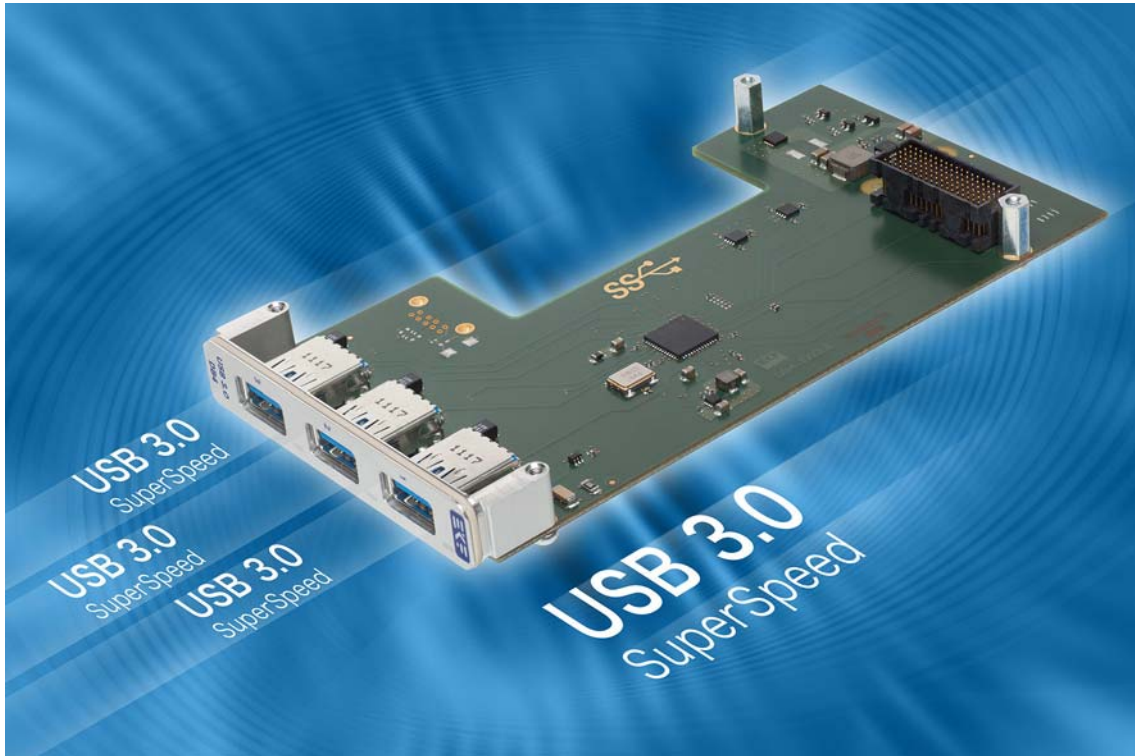
Complete circuit diagrams for this product are available for customers on request. Signing of a non-disclosure agreement would be needed. Please contact [sales@ekf.de](mailto:sales@ekf.de) for details.

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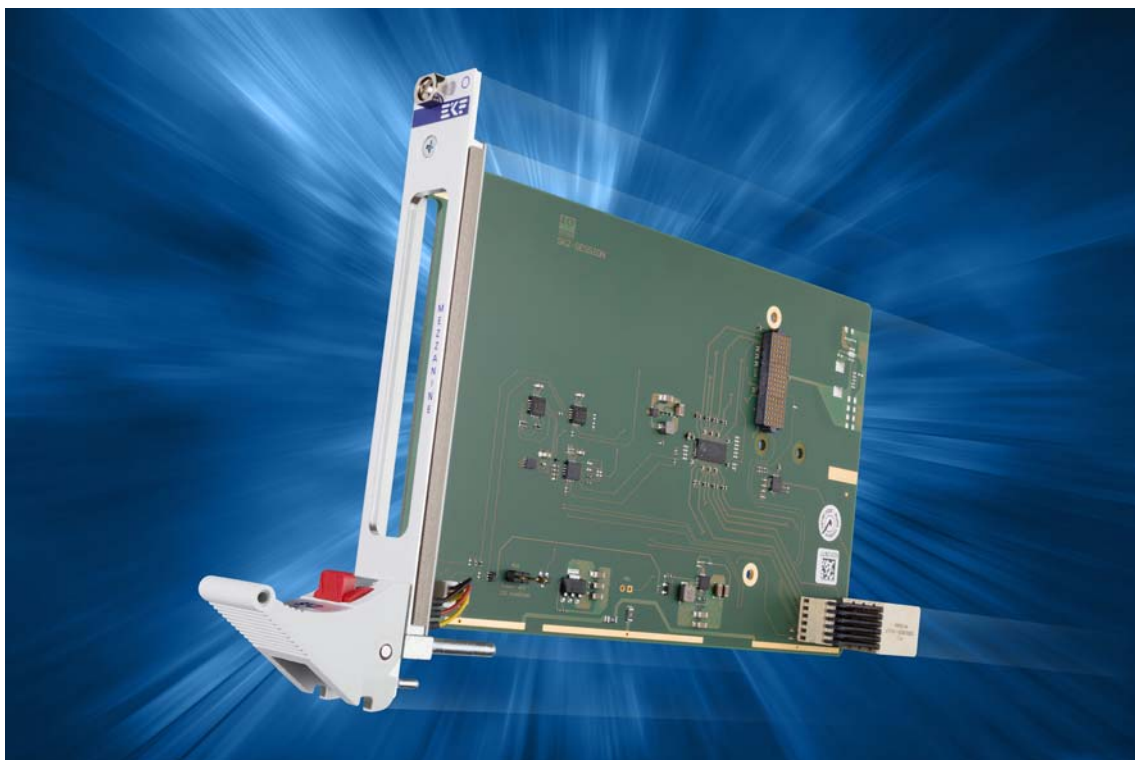


DU1-MUSTANG XMC Module • Isolated RS-485





DB4-EAGLE XMC Module • USB 3.0



SK2-SESSION • CompactPCI Serial XMC Module Carrier



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