Technical Information

CCI-RAP

Mezzanine I/O Expansion Board

Dual PCI Express Mini Card Sockets & SATA Controller

Document No. 4794 • Ed. 9 • 2009-03

CCI-RAP with C20-SATA

Contents

About this Manual

This manual is a short form description of the technical aspects of the CCI-RAP, required for installation and system integration. It is intended for the advanced user only.

Edition History

EKF Document	Ed.	Contents/*Changes*	Author	Date
Text # 4794 cci_tie.wpd	1	Technical Information CCI-RAP English, Preliminary Edition	jj	30 August 2007
	2	Added illustration 'Power Distribution'	jj	4 September 2007
	3	Secondary SIM card holder	jj	25 September 2007
	4	P-SATA2/3 added to block diagram	jj	22 November 2007
	5	Updated 'Concept Drawing' (C20-SATA outlines)	jj	15 February 2008
	6	Major document review	jj	10 March 2008
	7	Changed assignment COM-A / COM-B	hg	11 June 2008
	8	Added images	jj	17 November 2008
	9	Added images of sample GSM/GPS and WLAN PCIe Mini Cards	jj	3 March 2009

Related Documents

For a description of the CCG-RUMBA or CCM-BOOGIE CPU cards, which may act as carrier board with respect to the CCI-RAP, please refer to the correspondent CPU user guide, available by download from www.ekf.com/c/ccpu/ccg/ccg_e.html or www.ekf.com/c/ccpu/ccm/ccm_e.html (change path accordingly for other CPU cards).

Nomenclature

Signal names used herein with an attached '#' designate active low lines.

Trade Marks

Some terms used herein are property of their respective owners, e.g.

- Intel, Pentium, Celeron, Pentium M, Core 2 Duo, Merom, Penryn, iAMT: ® Intel
- Santa Rosa Platform, Crestline Chipset GM965, Matanzas CRB: Intel
- ***CompactPCI®*** : ® PICMG
- Windows XP, Windows Vista: ® Microsoft
- EKF, ekf system: ® EKF

EKF does not claim this list to be complete.

Legal Disclaimer - Liability Exclusion

This manual has been edited as carefully as possible. We apologize for any potential mistake. Information provided herein is designated exclusively to the proficient user (system integrator, engineer). EKF can accept no responsibility for any damage caused by the use of this manual.

Standards

Specifications/Standards	
PCIe Mini Card	PCI Express™ Mini Card Electromechanical Specification Revision 1.1 March 28, 2005 (PCI SIG www.pcisig.com)
SATA	Serial ATA 2.5/2.6 Specification (www.sata-io.org)
CompactPCI	PICMG 2.0 (www.picmg.org)
PCI Local Bus	PCI 2.2/2.3/3.0 Standards (PCI SIG www.pcisig.com)
USB	Universal Serial Bus Revision 2.0 specification (www.usb.org/developers)
PCI Express	PCIe Base Spec. 1.1 and other (PCI SIG www.pcisig.com)
1394 FireWire	IEEE 1394a-2000 (standards.ieee.org)
CompactFlash	CF+ and CompactFlash Specification Revision 3.0 (www.compactflash.org)
DVI	Digital Visual Interface Rev. 1.0 (Digital Display Working Group www.ddwg.org)
TPM	Trusted Platform Module 1.2 (https://www.trustedcomputinggroup.org)

CCI-RAP Features

Feature Summary	
Form Factor	Single size Eurocard (160x100mm^2), needs 4HP (20.3mm) additional mounting space, typically delivered as a ready to use assembly unit including the CCG-RUMBA providing a common 8HP front panel shared with the CPU board, mounting position right (on top of CPU board)
PCIe Usage	▸ 2 Lanes for PCIe Mini Card sockets (1 each) ▸ 1 Lane dedicated to SATA/PATA controller ▸ 1 Lane dedicated to IEEE 1394a controller
PCIe Mini Card	▸ 2 x PCI Express Mini Card sockets ▸ Socket 1 UIM port wired to on-board SIM connector (hinge style) ▸ Socket 2 UIM port wired to J1 connector (rear I/O option) ▸ Suitable for WLAN, GSM, Turbo Memory and other PCIe Mini Cards
SATA/PATA [3]	SMB363, PCIe to 2 x SATA II / 1 x PATA controller
1394a FireWire [3]	XIO2200A, PCIe to 1394a bridge, dual cable port 400Mbps (100/200/400)
USB Solid State Drive	Pin header provided for low profile industrial USB SSD module, e.g. Intel, M-Systems, STEC (8GB as of current)
LPC Super-I/O [3] (SIO2)	SCH3114, parallel port, 4 serial ports, PS/2 keyboard & mouse port, LPC interface
Firmware Hub [3] (FWH2)	82802 generic device, 8Mbit Flash, LPC interface, can be switched as secondary or primary (boot code) FWH
COM Port Serial Transceivers [3]	Up to 2 x ADM211 or equivalent, EIA/TIA-232E (RS-232E) 230kbps max.
DVI [3]	SDVO to DVI (Digital Visual Interface) PanelLink/TMDS transmitter, dual screen operation (together with the carrier boards primary DVI video output), DVI is a stuffing option (front panel DVI connector replaces upper COM D-Sub connector)
TPM [3]	Option Trusted Platform Module cryptographic chip according to TPM 1.2
Front Panel Connectors [1]	▸ 2 x FireWire 1394a receptacles ▸ 2 x RS-232E male D-Sub COM port connectors (1 x if DVI is provided) ▸ 1 x Antenna output (cable from PCIe Mini Card) - WLAN or GSM ▸ 1 x DVI receptacle (option, replaces 1 x COM D-Sub connector)
Host I/F Connectors (to CCG-RUMBA CPU Carrier Board) [1]	▸ PCI Express interface (PCIe x 4) ▸ Multifunction expansion interface (LPC, USB, SMB) ▸ SDVO (Serial Digital Video Out) port C graphics interface
On-Board I/O Connectors [1]	▸ 2 x PCI Express Mini Card Sockets (2 x SIM card socket in addition) ▸ Up to 3 x U.FL style receptacles, wired to SMA front panel antenna connectors ▸ Connector for attachment of optional C20-SATA mezzanine card with 1 or 2 SATA drives 2.5-inch (RAID capable) ▸ Socket for C10-CFA/C30-PATA CompactFlash mezzanine module or 1.8-inch PATA Flash disk module (top mount) ▸ Socket for C17-CFA CompactFlash mezzanine module (bottom mount) ▸ USB SSD Module pin header (2.0mm pitch, low profile) ▸ 2 x serial port TTL level 2.0mm pitch header (suitable for EKF CU-series PHY-modules) ▸ Reset

Rear I/O Connector Option [1]	Optional J1/J2 2.0mm hard metric connectors (CompactPCI style with proprietary signal mapping) for custom specific transition module or backplane, major signal groups: ▸ Parallel Port (LPT) ▸ COM ports 3 & 4 (TTL-level signals) ▸ PS/2 keyboard & mouse ▸ GPIO ▸ UIM ports from Mini Card 1 & 2 (external SIM card socket option) ▸ SMBus ▸ SATA (option)
On-Board Functions	Speaker, LEDs, SMBus EEPROM, temperature sensors
Mass Storage Options [2]	▸ C20-SATA mezzanine card with 1 or 2 SATA drives 2.5-inch (RAID capable) optional on-board ▸ C10-CFA or C30-PATA (top mount), or C17-CFA (bottom mount) CompactFlash, or 1.8-inch hard disk, or 1.8-inch SSD mezzanine module ▸ USB Solid State Disk (SSD) low profile module ▸ Intel® Turbo Memory (formerly Robson)
Thermal Conditions [4] Environmental Conditions [4]	▸ Operating temperature: 0°C ... +70°C ▸ Storage temperature: -40°C ... +85°C, max. gradient 5°C/min ▸ Humidity 5% ... 95% RH non condensing ▸ Altitude -300m ... +3000m ▸ Shock 15g 0.33ms, 6g 6ms ▸ Vibration 1g 5-2000Hz
EC Regulations	▸ EN55022, EN55024, EN60950-1 (UL60950-1/IEC60950-1) ▸ 2002/95/EC (RoHS)
MTBF	tbd

[1] Not all of these connectors may be present or functional on your actual CCI-RAP board. Assembly of these connectors is highly custom specific. Discuss your needs with EKF before ordering.

[2] Options may be exclusive, i.e. not necessarily concurrently present. Ask EKF for special solutions if required.

[3] Silicon/function may not be present on your actual CCI-RAP board. Assembly of components is highly custom specific. Discuss your needs with EKF before ordering.

[4] Hard disk option may require decrease

Short Description

Available as a mezzanine add-on companion board to the CCG-RUMBA and successor CPU cards, the CCI-RAP is provided with additional PCI Express driven I/O resources, such as PCIe Mini Card sockets, SATA and FireWire controllers.

Mass storage options include SATA, PATA and USB SSD devices. Optionally, a DVI connector allows for dual screen video operating mode.

Furthermore the CCI-RAP is equipped with common legacy I/O ports, e.g. RS-232. A secondary Firmware Hub can be configured as alternate- or backup-BIOS.

Another option available is the Trusted Platform Module according to TPM 1.2 for safety critical applications.

The PCI Express Mini Card sockets are especially useful for wireless applications such as WLAN, GSM (HSDPA), WiMAX, and even GPS. Up to three front panel SMA style connectors are available for direct attachment of swivel antennas.

Each Mini Card slot is provided with a SIM card holder, as required for GSM based services.

The CCI-RAP will be attached on top of the CPU carrier board, and typically shares its front panel with the host carrier (usually 8HP front panel width in total). Interconnection between the CCI-RAP I/O module and the CPU carrier board is achieved by several expansion connectors, which comprise the PCIe (PCI Express x 4), LPC (Low Pin Count) and SDVO interfaces.

As an option, the CCI-RAP is available with a mezzanine module (C20-SATA), which accommodates one or two 2.5-inch SATA hard disk drives (RAID option). Alternatively, either a CompactFlash card adapter, or a 1.8-inch Flash drive (or hard disk) can be attached to the CCI-RAP, as optional mezzanine module. In addition, a USB SSD (Solid State Drive) module can be stuffed.

Vision systems and other real time applications can profit from the dual port IEEE 1394a (FireWire) controller.

Sample GSM/GPS
PCIe Mini Card

Sample WLAN (WiFi)
PCIe Mini Card

CCI-RAP with C20-SATA Dual-Drive Module

CCI-RAP with Triple Antenna Connectors

The CCI-RAP communicates by means of 3 bottom mount expansion connectors with the host CPU: P-PCIE (PCI Express x 4), P-EXP (multi-function I/F such as LPC, USB, SMB), and P-SDVO (Serial Digital Video).

The PCI Express interface (P-PCIE) is comprised of 4 PCIe lanes, which are derived from the ICH component on the CPU carrier board. Each Mini Card socket requires a single PCIe lane, and the remaining two lanes are in use for the SATA/PATA controller and the IEEE 1394a controller.

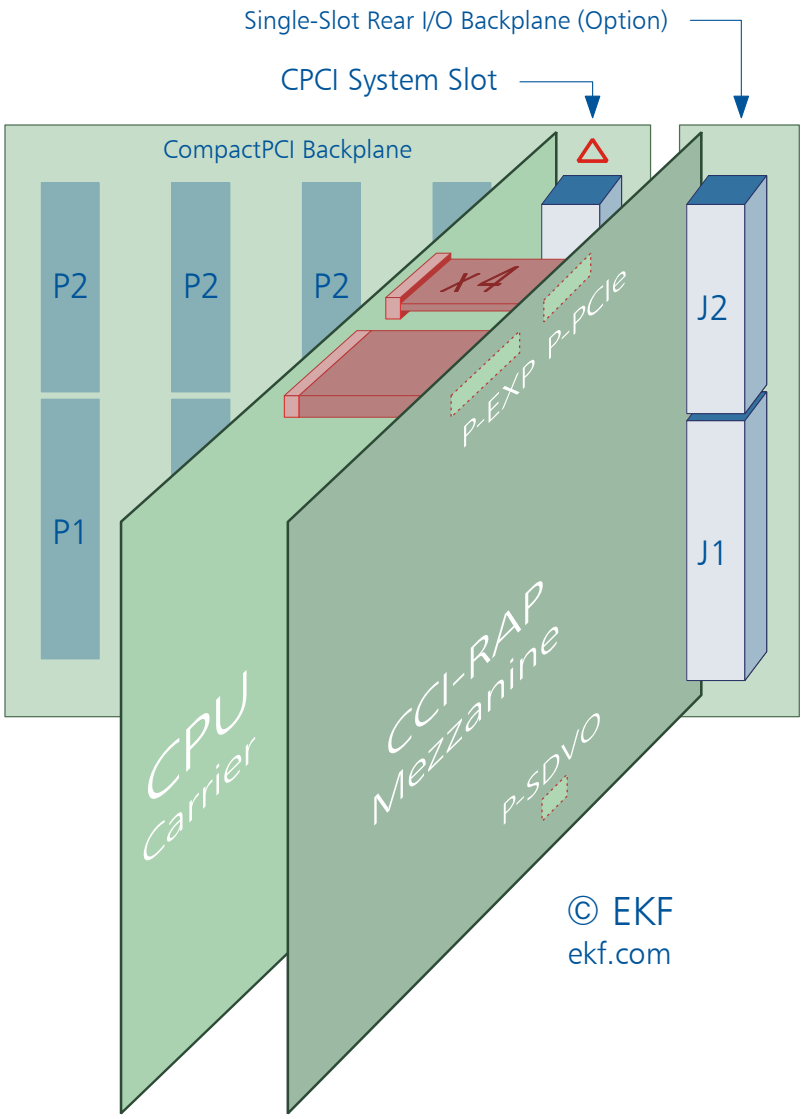
P-EXP combines several southbridge data channels: The LPC (Low Pin Count) is a multiplexed ISA bus, enabling the super-I/O (SIO) controller chip to emulate the legacy I/O interfaces; among these are the classic parallel (printer) and serial (COM) ports. Two USB lines are routed to the Mini Card sockets and the USB SSD connector. The SMB (System Management Bus) is an enhanced I^2C interface, enabling the BIOS and OS to gain access to special control functions of the PCIe clock buffer, the SATA controller and the Mini Cards. In addition, an EEPROM attached to the SMB is provided on the CCI-RAP, as configuration data storage.

A parallel ATA/IDE host interface connector towards the CCG-RUMBA is not required on the CCI-RAP, due to the combined on-board SATA/PATA controller. Within future Intel CPU chipset generations, the PATA/IDE will be completely omitted, hence this function has to be emulated on the side board.

The SDVO interface (P-SDVO) connects to the multiplexed PEG/SDVO graphics I/F of the GMCH (northbridge) on the CPU carrier board. The SDVO-C port is used to establish a secondary PanelLink (DVI) channel on the CCI-RAP, in addition to the primary DVI connector on the CCG-RUMBA. Basically, dual screen operation mode is also possible with the CCG-RUMBA alone. Due to the VGA signals on its DVI-I connector, a digital and in addition a VGA monitor can be attached simultaneously (splitter cable required). However, if two DVI (digital) monitors are mandatory, the CCI-RAP can be optionally ordered with a secondary PanelLink transmitter and DVI front panel connector.

The CCI-RAP fits on the top side of the CCG-RUMBA CPU board, which is on the right side when looking at the front panel of the boards while inserted into a CompactPCI rack. A suitable backplane provides its CPCI slots beginning with the CPU carrier board (CPCI system slot) from right to left. The CPCI system must provide additional mounting space to the right side for the CCI-RAP.

The Trusted Platform Module is an optionally available cryptographic chip, which provides a comprehensive hardware and software solution for safer computing. Conforming to the TPM1.2 standard of the TCG, the TPM is comprised of a 16-bit security controller and additional hardware e.g. to generate 2048 bit RSA keys and true random numbers, thus meeting the highest industry rating for digital security.



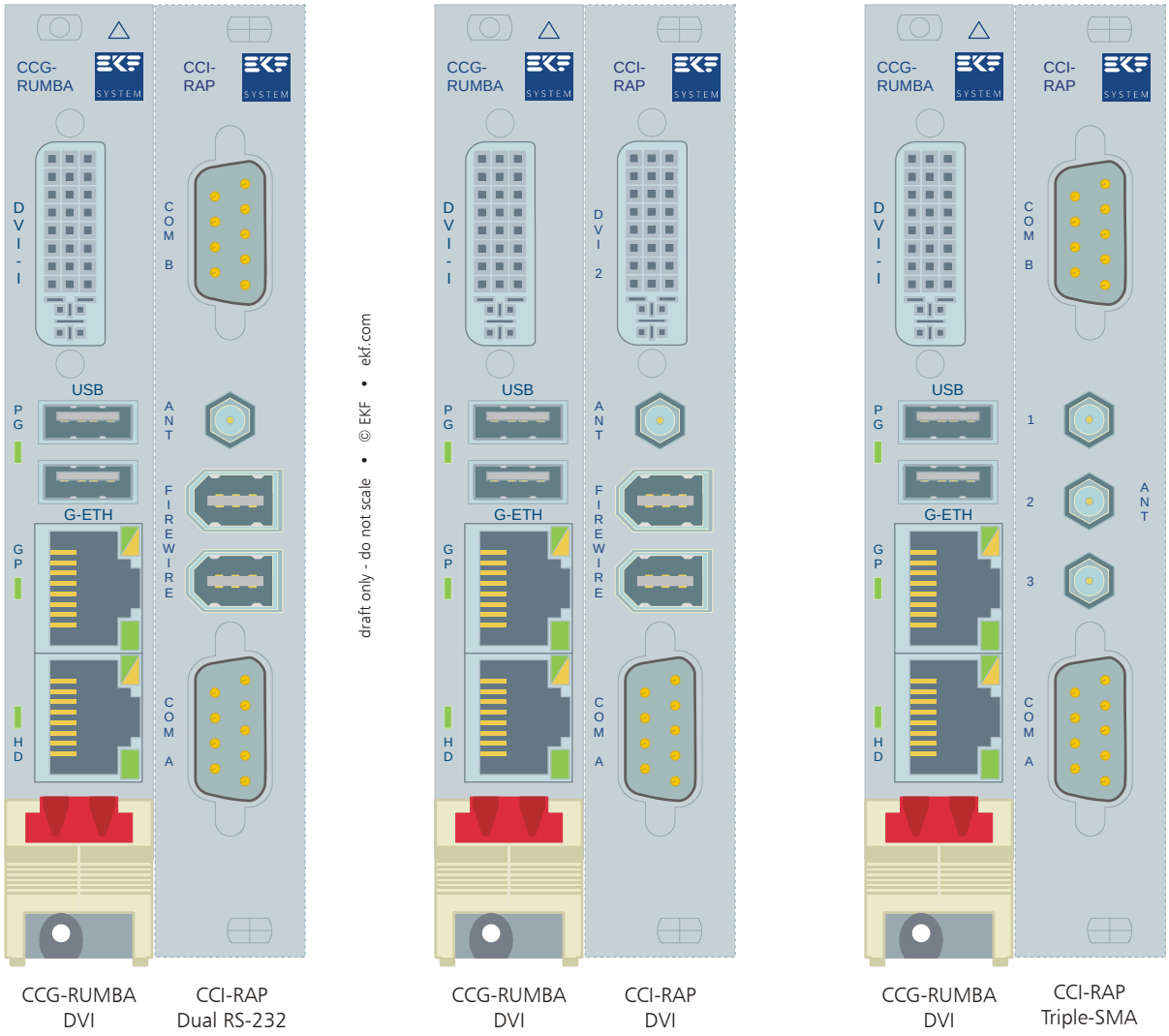
CCI-RAP on Top of the CPU Carrier

As of current, the suitable CPU carrier board for use together with the CCI-RAP mezzanine module is the CCG-RUMBA (and successors). The CCI-RAP expansion board mounts on top (at the right side) of the CCG-RUMBA.

If the CompactPCI backplane is provided with a right aligned system slot, be sure to position the CPU carrier board to the rightmost CPCI slot (and not the CCI-RAP). Consequently, the CCI-RAP then occupies the next card slot to the right, outside of the CPCI backplane, which may be provided with a single slot rear I/O P1/P2 backplane. In order to make use of the rear I/O capability of the CCI-RAP, its optional J1/J2 rear I/O connectors must be stuffed (consider before ordering). This assembly order (right aligned CPCI system slot) is preferred because no CompactPCI slot is lost for the CCI-RAP.

Vice versa, if a CPCI backplane is mandatory with a left aligned system slot, the CCI-RAP must not be equipped with J1/J2 connectors, and occupies a regular CompactPCI slot then. Of course, this assembly solution is not suitable for rear I/O with the CCI-RAP, and a CPCI slot will be lost. With J1/J2 stuffed, a coding key present on J1 would prevent insertion of the CCI-RAP into a CPCI card slot.

Front Panel Variations

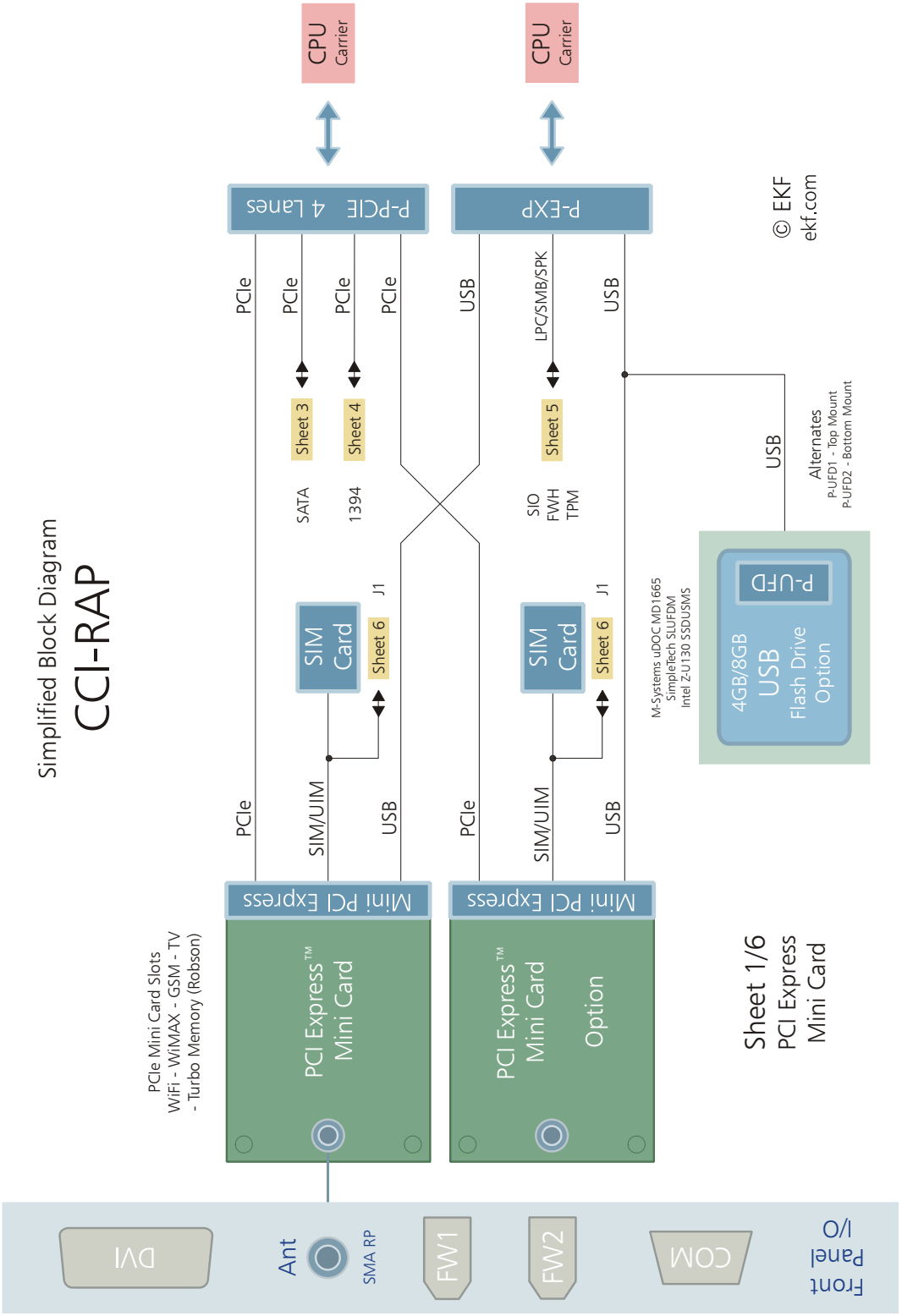


Typically the CCG-RUMBA carrier board CPU and the CCI-RAP share a common 3U/8HP front panel. The CCI-RAP is available in two flavours, either with dual COM port connectors, or with a DVI output, which replaces one COM port connector. Not shown in the illustration above are variations of the CCG-RUMBA (e.g. with VGA connector rather than DVI).

For wireless applications requiring more than one antenna (e.g. MIMO), EKF can provide modified CCI-RAP boards with a dual- or triple-antenna front panel. However, additional SMA jacks each replace a FireWire receptacle. The triple-antenna solution therefore is not equipped with a IEEE 1394 controller. As an alternate, a double-width custom specific front panel (8HP for CCI-RAP, 12HP in total together with CPU) can accommodate up to six additional SMA connectors (cable assembly U.FL to SMA bulkhead required).

EKF offers in addition custom specific design, for board electronics and also for front panel layout.

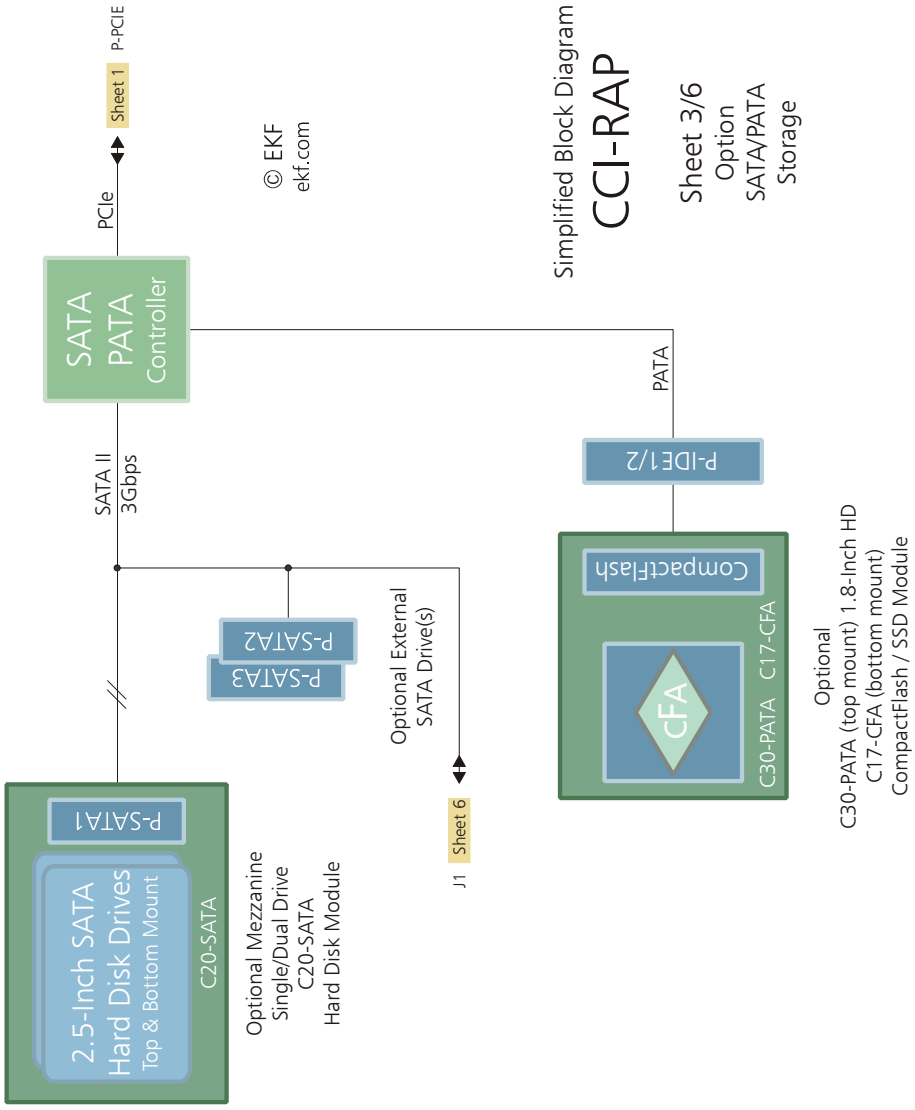
Block Diagram CCI-RAP

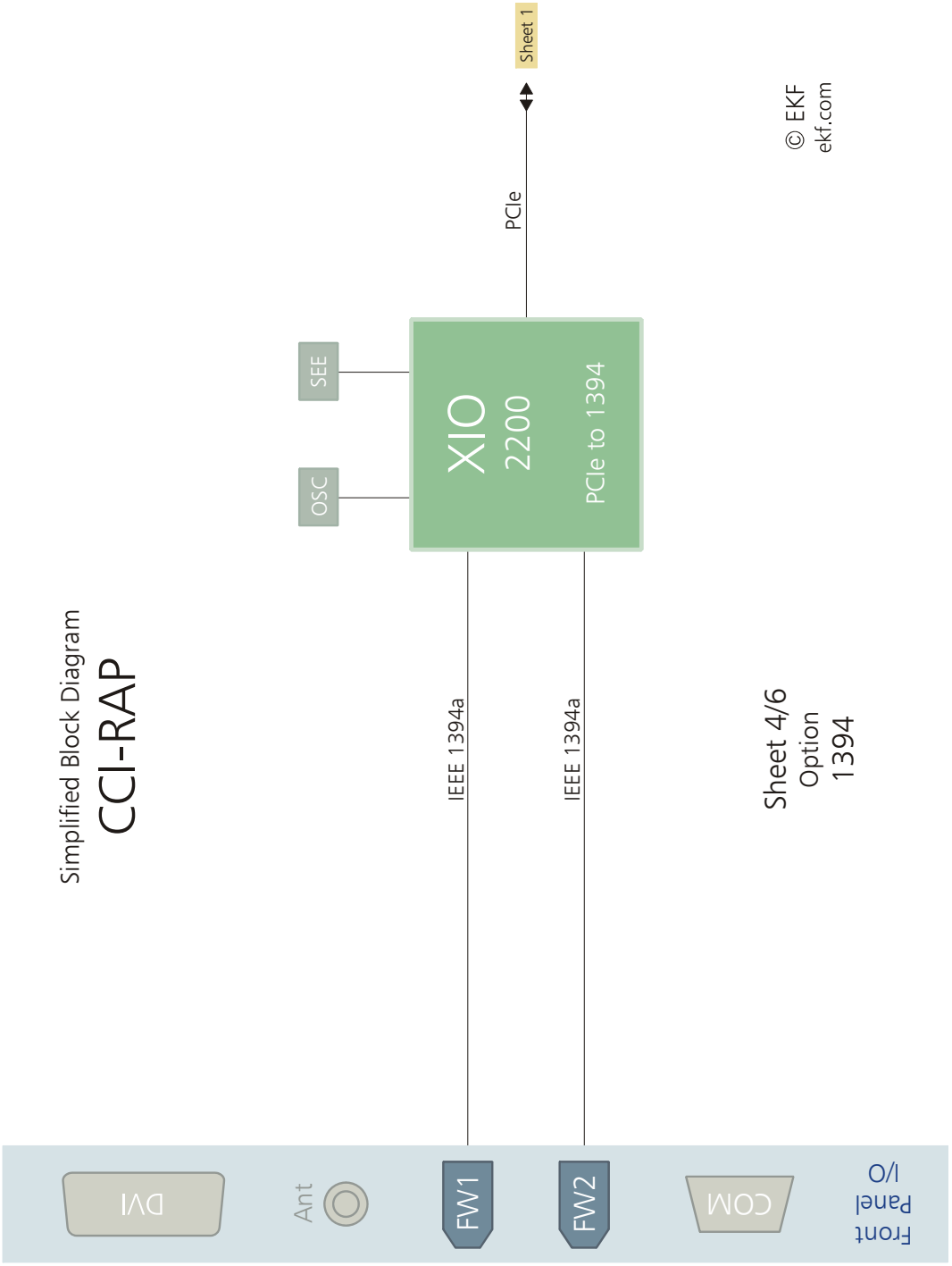


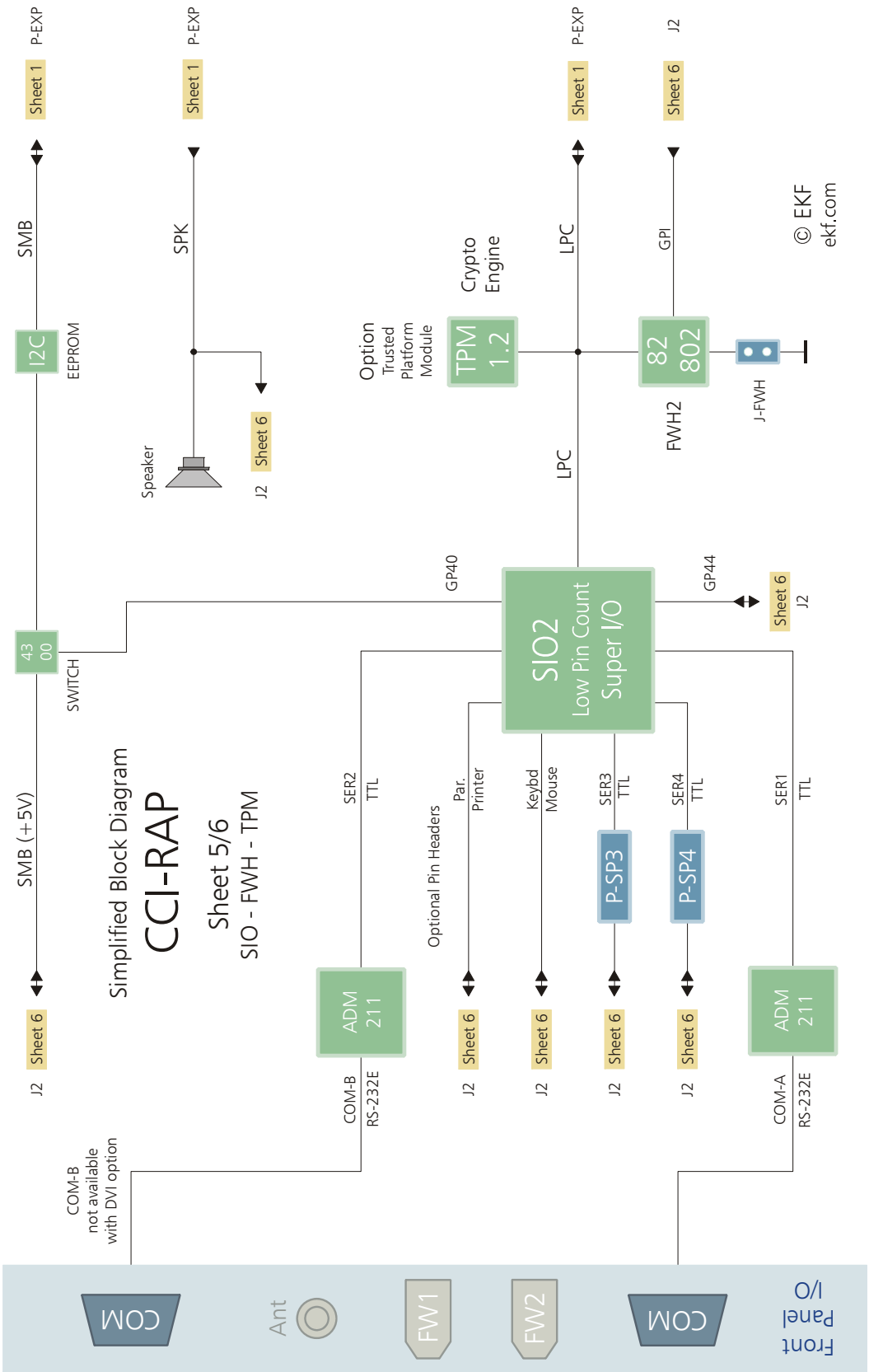
Simplified Block Diagram

CCI-RAP

Sheet 2/6
Option
Secondary DVI


Simplified Block Diagram
CCI-RAP
Sheet 3/6
Option
SATA/PATA
Storage
© EKF
ekf.com
P-PCIE
Sheet 1
PCIe
SATA
PATA
Controller
SATA II
3Gbps
PATA
P-IDE1/2
P-SATA2
P-SATA3
Optional External
SATA Drive(s)
J1
Sheet 6
CompactFlash
CFA
C30-PATA C17-CFA
Optional
C30-PATA (top mount) 1.8-Inch HD
C17-CFA (bottom mount)
CompactFlash / SSD Module
P-SATA1
2.5-Inch SATA
Hard Disk Drives
Top & Bottom Mount
C20-SATA
Optional Mezzanine
Single/Dual Drive
C20-SATA
Hard Disk Module


Simplified Block Diagram
CCI-RAP
Sheet 4/6
Option
1394
© EKF
ekf.com
Sheet 1
PCIe
XIO
2200
PCIe to 1394
SEE
OSC
IEEE 1394a
IEEE 1394a
Front
Panel
I/O
COM
FW1
FW2
Ant
DVI

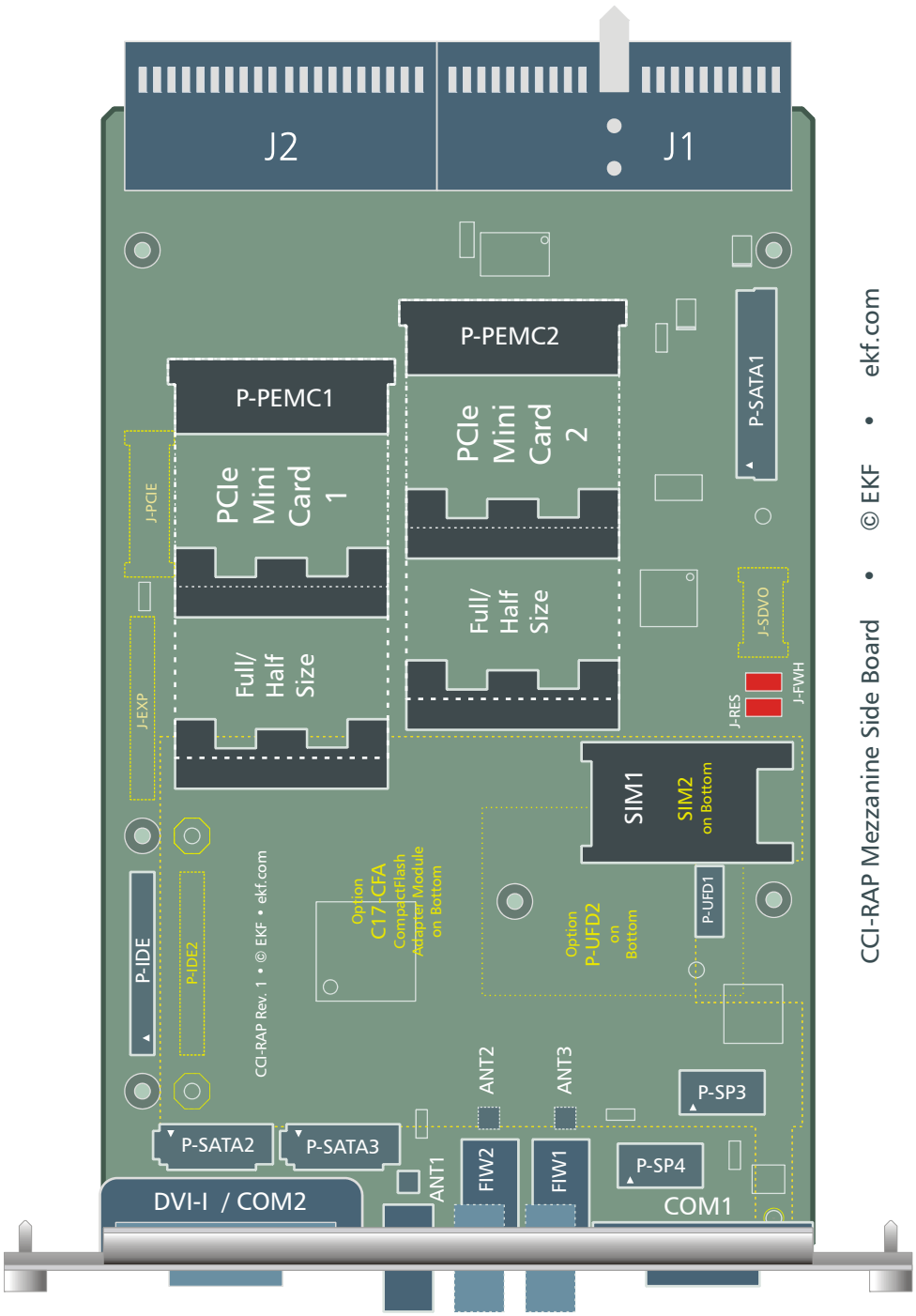

Simplified Block Diagram
CCI-RAP
Sheet 5/6
SIO - FWH - TPM
© EKF
ekf.com
P-EXP
Sheet 1
SMB
I2C
EEPROM
SPK
Speaker
J2
Sheet 6
Option
Trusted
Platform
Module
TPM
1.2
Crypto
Engine
LPC
GPI
82
802
FWH2
J-FWH
J2
Sheet 6
43
00
SWITCH
SMB (+5V)
GP40
SIO2
Low Pin Count
Super I/O
GP44
Sheet 6
J2
Optional Pin Headers
SER2
TTL
Par.
Printer
Keybd
Mouse
SER3
TTL
SER4
TTL
SER1
TTL
ADM
211
P-SP3
P-SP4
ADM
211
COM-B
RS-232E
COM-A
RS-232E
COM-B
not available
with DVI option
COM
Ant
FW1
FW2
COM
Front
Panel
I/O

Simplified Block Diagram

CCI-RAP

Sheet 6/6
J1 - J2
Rear I/O
Option

Top View Component Assembly CCI-RAP



Front Panel Connectors

ANT1 ANT2, ANT3 [3]	SMA style antenna connector, wired to U.FL style PCB receptacle, for U.FL cable harness from Mini Card antenna output to CCI-RAP PCB (not required for non wireless Mini Cards such as Turbo Memory), ANT2/3 available as an option
COM-A [1]	RS-232E serial communications port (CCI-RAP on-board SIO2 serial port 1), D-Sub 9-position male connector
COM-B [1 2]	RS-232E serial port (CCE on-board SIO2 serial port 2), D-Sub 9-position male connector
DVI [2]	Option Digital Video Port (DVI-D)
FW1 [3]	1394a FireWire receptacle, PHY port 1
FW2 [3]	1394a FireWire receptacle, PHY port 2

[1] Due to a primary SIO which may be present on the CPU board itself, the BIOS may assign COM port numbers different from COM1/COM2 to these interface lines on the CCI-RAP, e.g. COM2/COM3.

[2] If present, the DVI receptacle replaces the COM-A connectors, due to insufficient space on the front panel

[3] FireWire connector position(s) may be optionally replaced by additional SMA antenna connector(s)

On-Board Connectors

P-IDE1	Dual row socket, for top mount attachment of a CompactFlash socket or 1.8-inch Flash disk (or HD) on a mezzanine module (C10-CFA, C30-PATA)
P-IDE2	Dual row socket, for bottom mount attachment of a CompactFlash socket mezzanine module (C17-CFA)
P-PEMC1	PCI Express Mini Card socket & latch, for wireless applications and Turbo Memory, SIM card socket SIM1 corresponds to P-PEMC1
P-PEMC2	PCI Express Mini Card socket & latch, for wireless applications and Turbo Memory, optional SIM card socket SIM2 is assigned to P-PEMC2, in addition UIM signals of Mini Card 2 are available for rear I/O option
P-SATA1	Microspeed female connector, for top mount attachment of a C20-SATA mezzanine module, equipped with either one or two SATA drives 2.5-inch (RAID option with 2 drives)
P-SATA2 P-SATA3	Vertical latched SATA header, 7-position, stuffing option (exclusive to P-SATA1 and SATA via J1 rear I/O)
P-SP3/4 [1]	Pin headers 10-lead 2.00mm, provide TTL level serial COM port signals
P-UFD [2]	Socket 10-lead 2.00mm pitch, for low profile USB SSD (Solid State Drive)
SIM1	SIM card holder, hinge style, 6 contacts, GSM 11.11 Europe, corresponds with P-PEMC1
SIM2	SIM card holder, hinge style, 6 contacts, GSM 11.11 Europe, corresponds with P-PEMC2
UFL1-3	U.FL style (Hirose) receptacles, assigned to front panel antenna connectors ANT1-3

[1] Due to a primary SIO which may be present on the CPU board itself, the BIOS may assign COM port numbers different from COM3/COM4 to these interface lines on the CCI-RAP, e.g. COM4/COM5.

[2] USB channel shared (stuffing option) with P-PEMC2, so if assigned to P-PEMC2, P-UFD is not available

Jumpers

J-FWH [1]	Jumper 2.54mm, determines if the optional on-board firmware hub is acting as boot BIOS (jumper set) or as secondary BIOS (jumper removed = default).
J-RES [1]	Jumper 2.54mm, allows to force a CPU debug reset on the CCG-RUMBA carrier board

[1] Not all of these jumpers may be present or functional on your actual CCI-RAP board. Assembly of these jumpers is highly custom specific. Discuss your needs with EKF before ordering.

Inter-Board Connectors

P-EXP	Dual row socket, available from bottom of the CCI-RAP PCB, matching with the corresponding socket on the CPU carrier board, connected through a board stacker, comprising of: • LPC Low Pin Count interface • AC'97 Audio Codec / HD Audio (Azalia) • 2 x USB • SMB, Speaker, Reset
P-PCIE	High speed socket edge card connector, available from bottom of the CCI-RAP PCB, matching with the corresponding socket on the CPU carrier board, connected through a high speed strip line PCB (C22), comprising of: • Host CPU (ICH8) PCI Express (PCIe) x 4 interface
P-SDVO	High speed socket edge card connector, available from bottom of the CCI-RAP PCB, matching with the corresponding socket on the CPU carrier board, connected through a high speed strip line PCB (C21), comprising of: • Host CPU (GMCH 965) SDVO-C digital video

Rear I/O Connectors

J1 [2]	2.00mm brown keyed Hard Metric female connector, signal groups UIM I/F (SIM card) Mini Card 1 & 2, SATA
J2 [2]	2.00mm Hard Metric female connector, signal groups GPIO, parallel port, serial port 3 & 4 (TTL-level signals), SMB (+5V), speaker

[2] J1/J2 are optional

Please note:

Not all of the connectors or other elements listed above may be present or functional on your actual CCI-RAP board. Assembly of these connectors is highly custom specific. Discuss your needs (target application) with EKF before ordering, for an optimum board configuration.

Installing and Replacing Components

Before You Begin

Warnings

The procedures in this chapter assume familiarity with the general terminology associated with industrial electronics and with safety practices and regulatory compliance required for using and modifying electronic equipment. Disconnect the system from its power source and from any telecommunication links, networks or modems before performing any of the procedures described in this chapter. Failure to disconnect power, or telecommunication links before you open the system or perform any procedures can result in personal injury or equipment damage. Some parts of the system can continue to operate even though the power switch is in its off state.

Caution

Electrostatic discharge (ESD) can damage components. Perform the procedures described in this chapter only at an ESD workstation. If such a station is not available, you can provide some ESD protection by wearing an antistatic wrist strap and attaching it to a metal part of the system chassis or board front panel. Store the board only in its original ESD protected packaging. Retain the original packaging (antistatic bag and antistatic box) in case of returning the board to EKF for repair.

Installing the Board

Warning

This procedure should be done only by qualified technical personnel. Disconnect the system from its power source before doing the procedures described here. Failure to disconnect power, or telecommunication links before you open the system or perform any procedures can result in personal injury or equipment damage.

Typically you will perform the following steps:

- Switch off the system, remove the AC power cord
- Attach your antistatic wrist strap to a metallic part of the system 
- Remove the board packaging, be sure to touch the board only at the front panel
- Identify the related CompactPCI slot (peripheral slot for I/O boards, system slot for CPU boards, with the system slot typically most right or most left to the backplane)
- Insert card carefully (be sure not to damage components mounted on the bottom side of the board by scratching neighboured front panels)
- A card with onboard connectors requires attachment of associated cabling now
- Lock the ejector lever, fix screws at the front panel (top/bottom)
- Retain original packaging in case of return

Removing the Board

Warning

This procedure should be done only by qualified technical personnel. Disconnect the system from its power source before doing the procedures described here. Failure to disconnect power, or telecommunication links before you open the system or perform any procedures can result in personal injury or equipment damage.

Typically you will perform the following steps:

- Switch off the system, remove the AC power cord
- Attach your antistatic wrist strap to a metallic part of the system
- Identify the board, be sure to touch the board only at the front panel
- unfasten both front panel screws (top/bottom), unlock the ejector lever
- Remove any onboard cabling assembly
- Activate the ejector lever
- Remove the card carefully (be sure not to damage components mounted on the bottom side of the board by scratching neighboured front panels)
- Store board in the original packaging, do not touch any components, hold the board at the front panel only

Warning

Do not expose the card to fire. Battery cells and other components could explode and cause personal injury.

EMC Recommendations

CE

In order to comply with the CE regulations for EMC, it is mandatory to observe the following rules:

- The chassis or rack including other boards in use must comply entirely with CE
- Close all board slots not in use with a blind front panel
- Front panels must be fastened by built-in screws
- Cover any unused front panel mounted connector with a shielding cap
- External communications cable assemblies must be shielded (shield connected only at one end of the cable)
- Use ferrite beads for cabling wherever appropriate
- Some connectors may require additional isolating parts

Reccomended Accessories

Blind CPCI Front Panels	EKF Elektronik	Widths currently available (1HP=5.08mm): with handle 4HP/8HP without handle 2HP/4HP/8HP/10HP/12HP
Ferrit Bead Filters	ARP Datacom, 63115 Dietzenbach	Ordering No. 102 820 (cable diameter 6.5mm) 102 821 (cable diameter 10.0mm) 102 822 (cable diameter 13.0mm)
Metal Shielding Caps	Conec-Polytronic, 59557 Lippstadt	Ordering No. CDFA 09 165 X 13129 X (DB9) CDSFA 15 165 X 12979 X (DB15) CDSFA 25 165 X 12989 X (DB25)

Technical Reference - Connectors

Caution

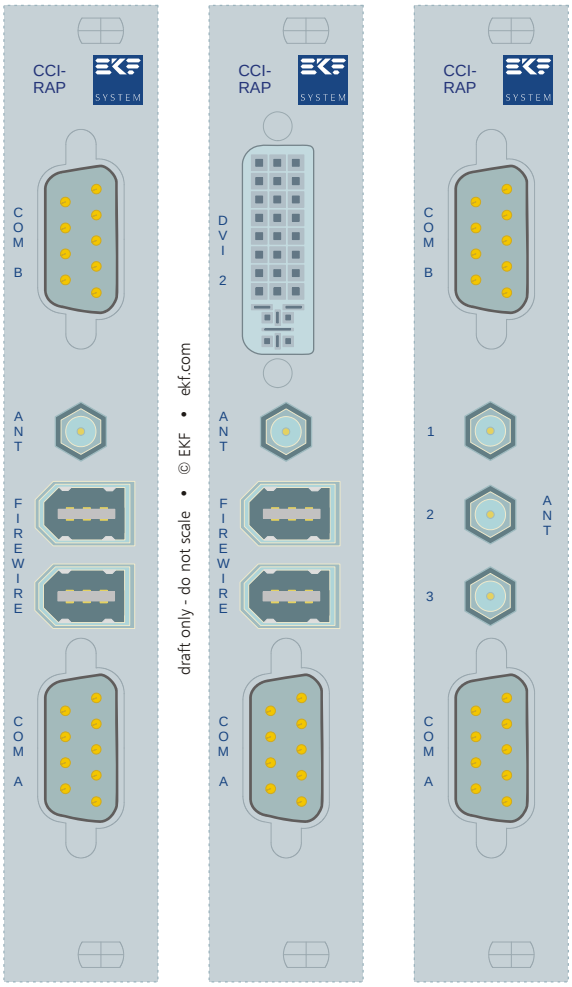
Some of the connectors may provide operating voltage (e.g. +12V, +5V and +3.3V) to devices inside the system chassis, such as internal peripherals. Not all of these connectors are overcurrent protected. Do not use these connectors for powering devices external to the computer chassis. A fault in the load presented by the external devices could cause damage to the board, the interconnecting cable and the external devices themselves.

Please Note

The CCI-RAP mezzanine module may be equipped with several on-board connectors for system internal usage. Not all of these connectors may be present on a particular board. Be sure to specify your individual needs when ordering the CCI-RAP board. Characteristic features and the pin assignments of each connector are described on the following pages (connector designation in alphabetical order within the groups 'front panel connectors', 'on-board connectors', 'inter-board connectors', and 'rear I/O connectors').

Front Panel Connectors

As of current, the suitable CPU carrier board for use together with the CCI-RAP mezzanine module is the CCG-RUMBA. The CCI-RAP side board mounts on top (at the right side) of the CCG-RUMBA. By default, the CCI-RAP shares an 8HP (~40.6mm) front panel with the CPU carrier board. Further more, custom specific front panel options are available on request. Shown below are three basic variants of the CCI-RAP (illustration w/o CCG-RUMBA front panel).



CCI-RAP
Dual RS-232

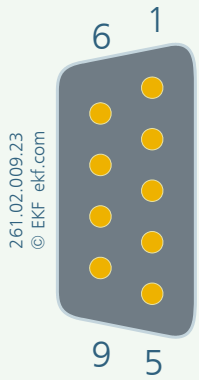
CCI-RAP
DVI

CCI-RAP
Triple SMA

COM-A/COM-B Serial Port Connectors

The on-board secondary Super-I/O (SIO) on the CCI-RAP provides four asynchronous serial interfaces, two of them available from the front panel (EIA/TIA 232), and another two as on-board pin headers or rear I/O only (TTL-level signals).

Due to another (primary) SIO typically available on the CCG-RUMBA host board, the serial interfaces are not necessarily assigned to the COM-1/COM-4 ports of a typical PC. Verify or modify the accompanying CCG-RUMBA BIOS settings for mapping of physical asynchronous serial I/O ports to the logical COM port order. Being ignorant of the actual port mapping, the serial port front panel connectors are marked neutrally as COM-A (lower connector) and COM-B (upper connector).

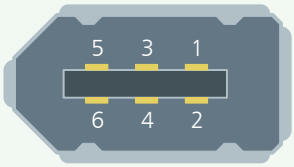
COM-A/B RS-232 Male D-Sub 9 261.02.009.23				
			1	DCD1(2)
	DSR1(2)	6		
			2	RXD1(2)
	RTS1(2)	7		
			3	TXD1(2)
	CTS1(2)	8		
			4	DTR1(2)
	RI1(2)	9		
			5	GND

The on-board ESD protected RS-232E transceivers on the CCI-RAP allow a bitrate of up to 230kbps.

If a DVI receptacle is provided on the CCI-RAP, the upper COM connector will be removed.

1394 FireWire Connectors

The CCI-RAP is equipped with an integrated PCIe to PCI bridge and 1394a OHCI compliant LLC/PHY (XIO2200A). Both cable port connectors are suitable for data transfer rates of 100Mbps, 200Mbps and 400Mbps according to IEEE1394a-2000.

2 x 1394a FireWire Receptacles 270.30.06.1		
 1394a FireWire Receptacle © EKF • ekf.com Part No. 270.30.06.1	1	+12V/0.5A Bus Power [1]
	2	GND
	3	TP B-
	4	TP B+
	5	TP A-
	6	TP A+

[1] protected by PolySwitch resetable fuses 0.5A, sourced from +12V_CR (carrier board) and +12V_EXT (rear I/O optional connector J1), whatever voltage is higher

The cable port bus power (+12V nominal) on a particular FireWire receptacle is present if sourced across either

- the rear I/O optional connector J1 with attached power supply (+12V_EXT pin)
- the inter-board connector P-EXP pin 40
- the neighboured FireWire receptacle, if a self-powered 1394 device is attached to it

Both cable ports are fused by individual 0.5A PolySwitches (self resettable fuse). Due to a reasonable voltage drop across Schottky diodes in the 12V power lines, the actual bus power voltage may be as low as ~11.5V.

Typical operating systems provide software drivers for TIs FireWire components. If required, e.g. for GPIO programming, the XIO2200A data manual can be obtained from the www.ti.com website.

As an option, the CCI-RAP front panel can be equipped with a maximum of two additional SMA antenna connectors (three in total). Each additional SMA jack however would displace a FireWire receptacle.

Antenna Connector(s)

Wireless PCI Express Mini Cards (WLAN, WiMAX, GSM) require an *external* antenna, due to the metal (shielding) CompactPCI encasement. Popular WLAN antennas are available with a reverse polarity (RP) SMA plug (FCC part 15 compliant). The CCI-RAP therefore is equipped with the mating SMA RP 50 Ohm front panel jack (PCB mount, isolated from F/P). Hence an external angled/swivel antenna may be attached directly to the front panel SMA connector. Suitable antennas are available e.g. from Linx (www.linxtechnologies.com), or Pulse (www.pulseeng.com), for a variety of applications.

Typically, wireless Mini Cards are provided with the Hirose U.FL-R-SMT radio frequency connector, which requires as mating cable connector the Hirose U.FL-LP. Hence a short (~10cm), dual ended U.FL-LP style cable harness is needed in addition for strapping, from the particular Mini Card RF output, to the U.FL receptacle near the CCI-RAP antenna connector position(s). Please do not forget to order suitable cable assemblies, either directly from Hirose (www.hirose.com), or from EKF.

As an alternative, a single ended U.FL cable assembly can be replenished with a suitable bulkhead front panel connector, SMA or other style, which requires that the CCI-RAP on-board SMA connector is not populated or removed, or a wider custom specific front panel will be used. Such cable assemblies are available e.g. from ES&S (www.esskabel.de). The antenna connector has to be fixed to the CCI-RAP front panel by a nut (F/P cut-out must be suitable dimensioned). Thus, without using additional isolation parts, the antenna ground and the CompactPCI chassis (shield/earth) would be tied together. This may be tolerable for most applications, however EKF recommends utilization of the isolated on-board SMA connector whenever possible.

Due to the limited CCI-RAP front panel space, basically only one antenna connector may be provided. If additional RF connectors are mandatory (e.g. MIMO cards, or WLAN & GSM concurrent operation), up to 2 more SMA connectors can be stuffed (3 in total). Each additional SMA connector however replaces one FireWire receptacle.

A custom specific front panel and PCB board layout can be discussed with EKF (sales@ekf.de).

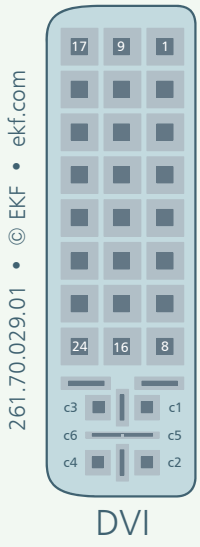
DVI-2 Receptacle

As an option, the CCI-RAP is available with a SDVO to PanelLink transceiver for digital video. The secondary DVI receptacle on the CCI-RAP can be used in addition to the primary DVI connector on the CCG-RUMBA for dual digital screen operation mode.

Other than with the CCG-RUMBA, the DVI connector on the CCI-RAP does not provide analog signals (VGA) in addition. Please understand that the CCI-RAP complies with DVI-D, though the actual front panel receptacle may contain (not connected) additional leads conforming to DVI-I. This allows usage of both DVI-D and DVI-I cable harnesses.

If the DVI option was chosen, the connector COM-B will be removed.

DVI Connector 261.70.029.01



DVI

17	TX0-	9	TX1-	1	TX2-
18	TX0+	10	TX1+	2	TX2+
19	GND	11	GND	3	GND
20		12		4	
21		13		5	
22	GND	14	DDC_POW [1)]	6	DDC_SCL
23	TXC+	15	GND	7	DDC_SDA
24	TXC-	16	DVI_HP	8	VSYNC

c3	BLUE	c1	RED
c6	GND	c5	GND
c4	HSYNC	c2	GREEN

[1)] +5V protected by a PolySwitch Fuse 1.5A

On-Board Connectors

The CCI-RAP can be equipped with several on-board connectors. Some of these connectors are available as an option only or exclusive to each other, and therefore may not be functional or even present on your actual board.

Assembly of these connectors is highly custom specific. Discuss your needs with EKF before ordering, so that the optimum board configuration for your application will be chosen.

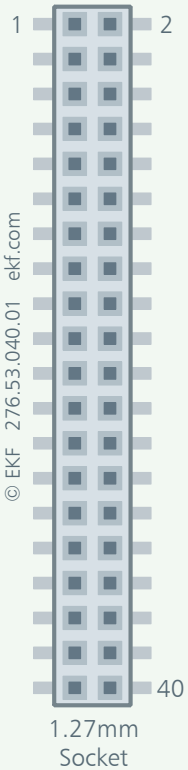
P-IDE1 P-IDE2

The CCI-RAP is provided with the JMB363 PCIe to SATA/PATA bridge. The PATA (IDE) signals are routed to the sockets P-IDE1, P-IDE2, and in addition to the optional connectors P-IDE3 and J1, in this order. A maximum of two devices (primary/secondary) can be attached to the IDE connectors. Stubs must be avoided on the IDE bus. Thus, if no external device(s) are connected to P-IDE3 and/or across J1, the IDE bus should end at P-IDE2. This is achieved by a set of zero Ohm resistor arrays on the IDE bus (RNI11-RNI18), located between P-IDE2 and P-IDE3. These resistors should not be stuffed if usage of P-IDE3 or rear I/O IDE across J1 is definitely not intended.

P-IDE1, if stuffed, is an optional top mount connector which is suitable to accommodate the optional C10-CFA mezzanine module, equipped either with a CompactFlash socket or an 1.8-inch PATA Solid-State Disk (SSD).

P-IDE2, if populated, is an optional bottom mount connector, suitable for a bottom mount CompactFlash mezzanine module (C17-CFA).

P-IDE1 / P-IDE2 CompactFlash/IDE Expansion Interface 1.27mm Socket 2 x 20 (276.53.040.01)

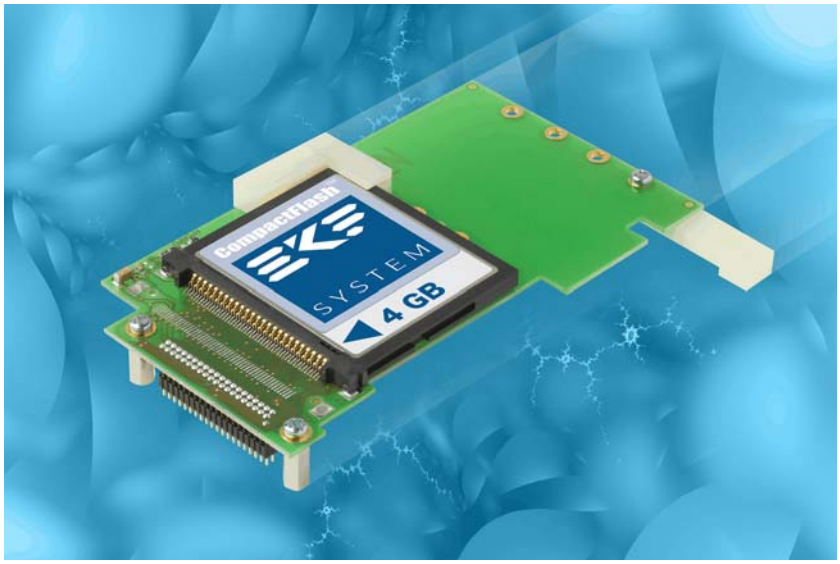


top view pin numbering order (P-IDE1)

IDE0_RESET#	1	2	GND
IDE0_DD07	3	4	IDE0_DD08
IDE0_DD06	5	6	IDE0_DD09
IDE0_DD05	7	8	IDE0_DD10
IDE0_DD04	9	10	IDE0_DD11
IDE0_DD03	11	12	IDE0_DD12
IDE0_DD02	13	14	IDE0_DD13
IDE0_DD01	15	16	IDE0_DD14
IDE0_DD00	17	18	IDE0_DD15
GND	19	20	+3.3V_CR *
IDE0_DMARQ	21	22	+3.3V_CR *
IDE0_DIOW#	23	24	GND
IDE0_DIOR#	25	26	GND
IDE0_IORDY	27	28	+5V_CR *
IDE0_DMACK#	29	30	+5V_CR *
IDE0_INTRQ	31	32	GND
IDE0_DA1	33	34	IDE_CBLID#
IDE0_DA0	35	36	IDE0_DA2
IDE0_CS0#	37	38	IDE0_CS1#
IDE0_ACT#	39	40	GND

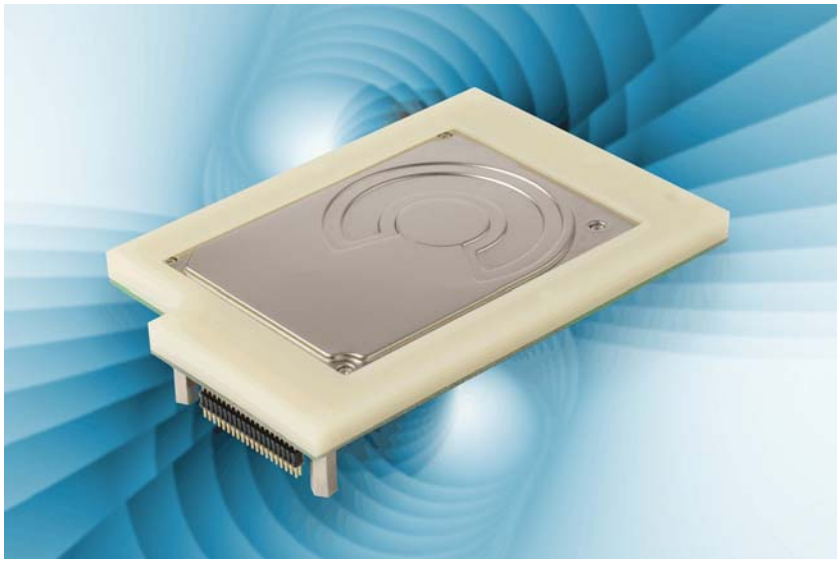
* switched power supply lines from CCG-RUMBA carrier board according to Sx state

P-IDE1 suitable for C10-CFA or C30-PATA module (top mount)
P-IDE2 suitable for C17-CFA module (bottom mount)

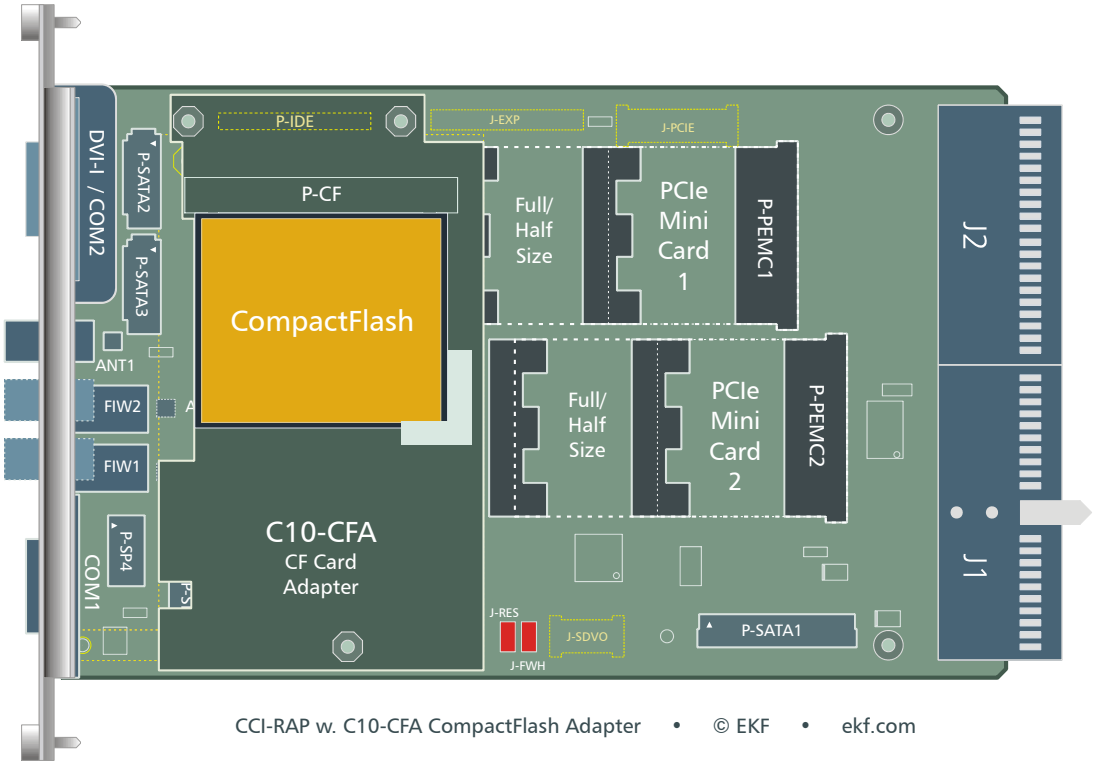


C10-CFA (Top Mount)

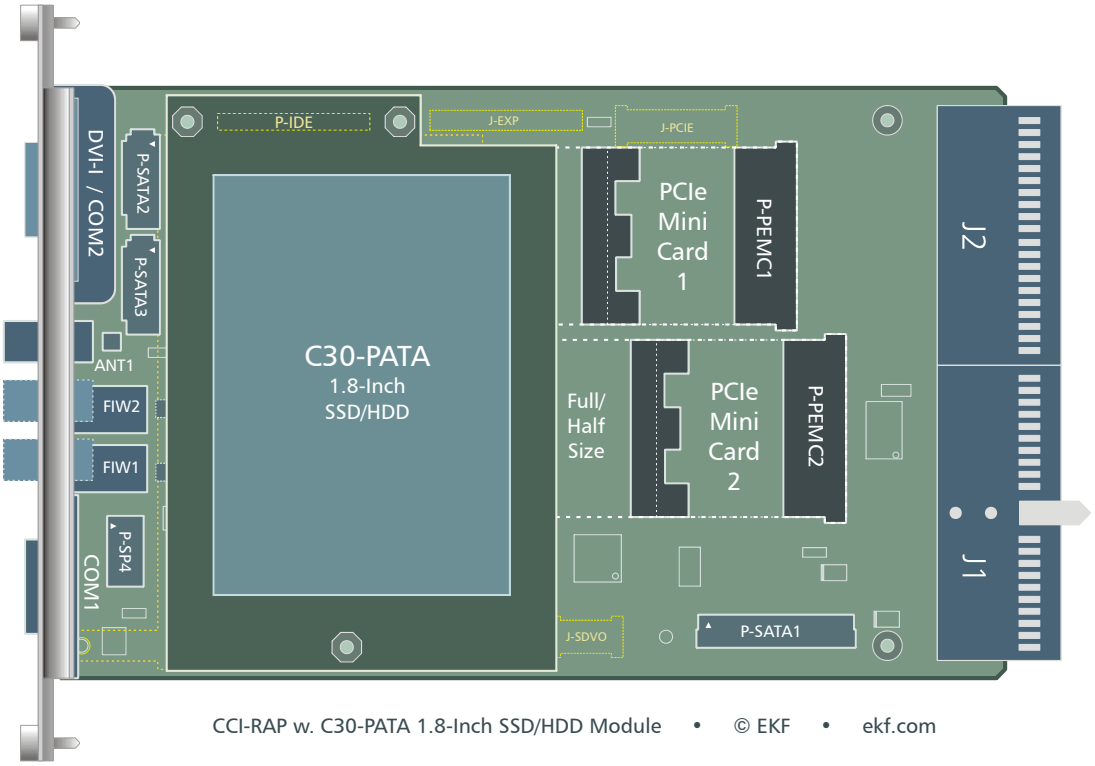
C17-CFA (Bottom Mount)



C30-PATA 1.8-Inch SSD (Top Mount)



CCI-RAP w. C10-CFA CompactFlash Adapter • © EKF • ekf.com



CCI-RAP w. C30-PATA 1.8-Inch SSD/HDD Module • © EKF • ekf.com

P-PEMC1 P-PEMC2

As an option, two sockets are provided for PCI-Express Mini Cards (e.g. such as wireless cards or Turbo Memory). For GSM telephone modules, on-board SIM card holders are associated with P-PEMC1 and P-PEMC2, in addition.

By specification*, the PCIe Mini Card sockets do not provide pins for the RF output of a wireless module, thus a cable assembly is required in addition, running from the Mini Card antenna output connector, to the U.FL style receptacle(s) assigned to the CCI-RAP front panel antenna connector(s) (for details refer to chapter Front Panel Connectors / Antenna). Due to space limitations in the standard front panel, a maximum of three antenna connectors is available (typically one only, as each additional SMA connector displaces a FireWire receptacle).

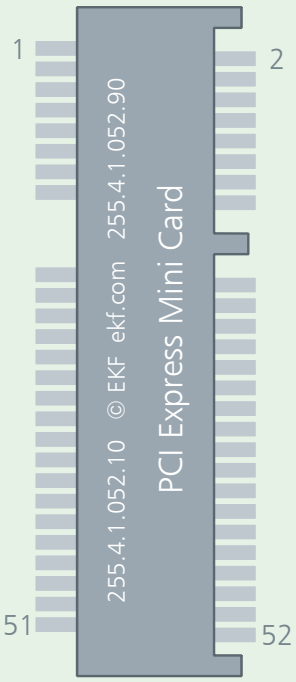
In future versions of the CCI-RAP, P-PEMC2 will provide in addition 3 proprietary signals, known as Intel® WiFi Link. This will allow for operation of the Intel® 4965AGN WLAN Mini Card as Intel® AMT (Active Management Technology) capable data path. The recommended socket position for iAMT enbled WLAN modules is P-PEMC2.

Both sockets P-PEMC1 and P-PEMC2 are equally suited for the so called Turbo Memory cache module Mini Card. Based on NAND Flash technology, employment of the Intel® Turbo Memory can improve system boot time and will deliver up to 2x faster performance when loading frequently used applications. Drivers can be downloaded from the Intel website (as of current Windows® Vista only).

The PCIe Mini Card specification provides USB connectivity in addition to PCIe. Older Mini Cards, such as GSM modems, in fact often use the USB port. Unfortunately, the CCI-RAP receives 2 USB channels from the CCG-RUMBA, but provides 3 potential USB target devices. Besides the P-PEMC1/2 connectors there is an USB Flash disk module optional connector P-UFD on the CCI-RAP, which shares its USB port with the P-PEMC2 connector. A set of zero Ohm resistors can be stuffed to assign this USB channel either to P-PEMC2 or P-UFD. However, with modern designs such as the Intel® 4965AGN WLAN Mini Card or Intel® Turbo Memory attached to P-PEMC2, USB is not at all required for operation (both modules use PCI Express connectivity), so that P-PEMC2 can be used concurrently to P-UFD in many cases.

* PCI-SIG PCI Express Mini Card Electromechanical Specification, Rev.1.1

P-PEMC1 P-PEMC2
PCI Express Mini Card Socket (255.4.1.052.10) & Latch (255.4.1.052.90)

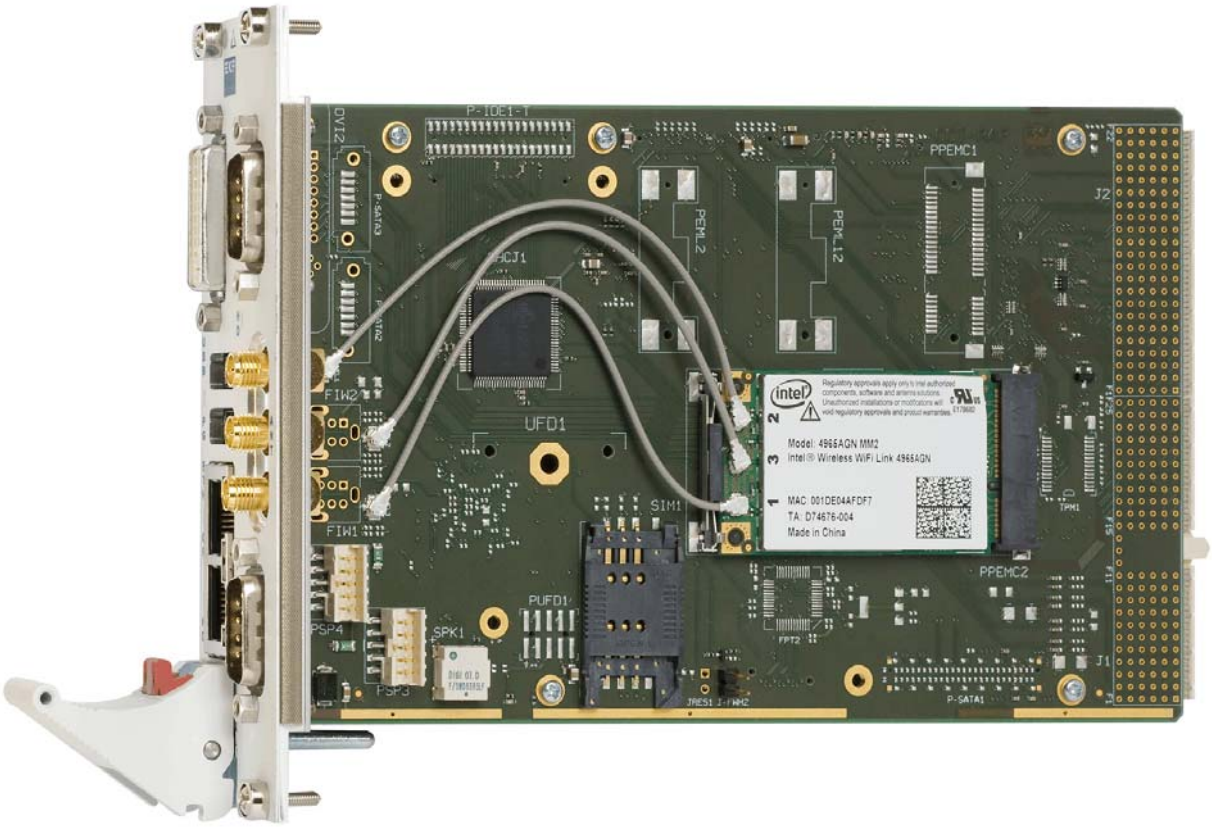


PE_WAKE#	1	2	+3.3V_CR
NC *BT_DATA*	3	4	GND
NC *BT_CHCLK*	5	6	+1.5V_MC*
CLKREQ_MC*#	7	8	PEMC*_UIM_C1
GND	9	10	PEMC*_UIM_C7
CKN_MC*	11	12	PEMC*_UIM_C3
CKP_MC*	13	14	PEMC*_UIM_C2
GND	15	16	PEMC*_UIM_C6
NC	17	18	GND
NC	19	20	WDIS_MC*#
GND	21	22	MINICARD_RST#
PE2_RN (PE3_RN)	23	24	+3.3V_CR
PE2_RP (PE3_RP)	25	26	GND
GND	27	28	+1.5V_MC*
GND	29	30	SMB_CLK
PE2_TN (PE3_TN)	31	32	SMB_DAT
PE2_TP (PE3_TP)	33	34	GND
GND	35	36	USBN_MC*
NC	37	38	USBP_MC*
NC	39	40	GND
NC	41	42	LED_WWAN_MC*
NC	43	44	LED_WLAN_MC*
Intel WiFi Link CLK ** *NC*	45	46	LED_WPAN_MC*
Intel WiFi Link DAT** *NC*	47	48	+1.5V_MC*
Intel WiFi Link RST#** *NC*	49	50	GND
NC	51	52	+3.3V_CR

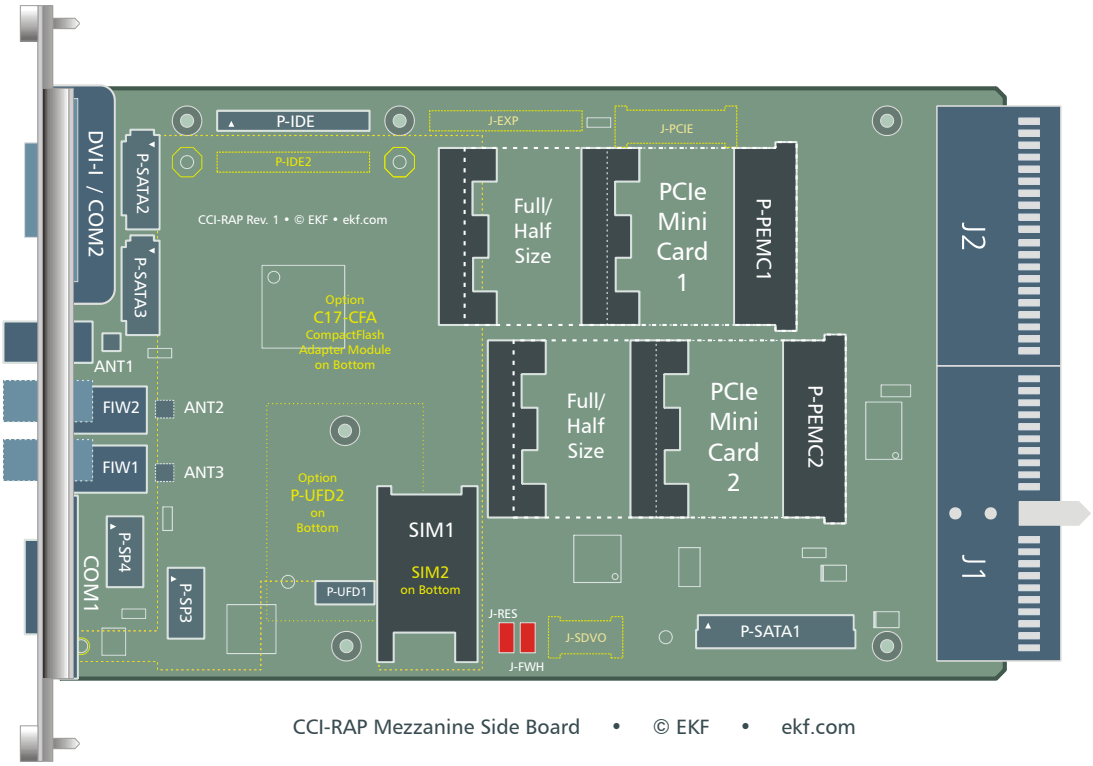
Notes:

Replace occurrences of * (single star) by either 1 (P-PEMC1) or 2 (P-PEMC2). WDIS_MC1# can be optionally controlled by SIO GP15 (serial port 3 DTR#), WDIS_MC2# is likewise tied to GP17 (serial port 3 RTS#). USB_MC2 is shared with the USB SSD connector P-UFD by stuffing option. PEMC1_UIM_Cx signals are wired to the on-board SIM card socket SIM1, while PEMC2_UIM_Cx signals are assigned to SIM2 and in addition available on J1 (rear I/O option).

** marked signals (WiFi Link) are an Intel proprietary extension to the PCIe Mini Card connector. These signals must match the ICH8M Controller Link 1 on the carrier board, for iAMT capability, and are available on the P-PEMC2 socket (future option).



Single PCIe Mini Card Socket, Triple Antenna for MIMO



CCI-RAP Mezzanine Side Board • © EKF • ekf.com

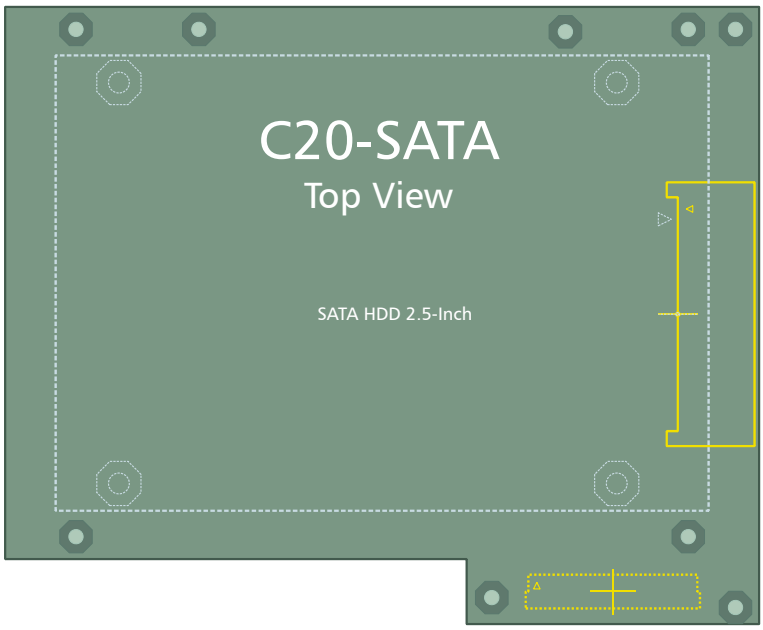
P-SATA1

The CCI-RAP is equipped with the JMB363 PCIe to single port PATA, dual port SATA controller (i.e. up to 4 mass storage devices in total). It provides two Serial ATA II channels, which are routed to the optional on-board connector P-SATA1. This is a high speed signals connector, suitable for attachment of the C20-SATA mezzanine module.

The C20-SATA is an optional storage module, which can be equipped with up to two 2.5-inch SATA drives, mounted back to back (one on top, one on bottom of the C20-SATA PCB).

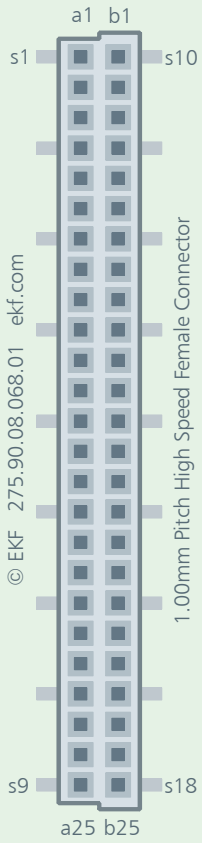
Typically, SATA drives require +5V as power source. The CCI-RAP takes this voltage either from the carrier CPU board (+5V_CR), which is a switched power line according to the S-state of the CPU, or as an alternative from the CCI-RAP rear I/O connector J1. Selection is done by CCI-RAP stuffing option, by means of a Polyswitch resettable 1.5A fuse populated on either one of the power lines. By default, +3.3V and +12V are not passed from the CCI-RAP to the C20-SATA mezzanine module - contact EKF if this is a requirement (available as stuffing option).

The JMB363 is a very popular SATA controller, which allows for several operating modes, including RAID 0, 1, 0+1. Drivers can be downloaded for Windows (WHQL certified) or Linux from ftp://driver.jmicron.com.tw, or alternate driver download portals such as www.pctweaker.net/category/treiber/chipsatz-treiber/jmicron or www.x-drivers.com/component/option,com_remository/func,select/id,4626/.



P-SATA1 is available as a stuffing option. There are two other SATA I/O variants available, P-SATA2 and P-SATA3 (7-position headers for attachment of latched SATA cables), or rear I/O via J1 (requires custom specific transition module). These options are provided only exclusive to each other - please select before ordering the CCI-RAP.

P-SATA1 SATA Expansion Interface 1.00mm Socket (275.90.08.068.01)



GND	a1	b1	GND
SATA0_TXP	a2	b2	
SATA0_TXN	a3	b3	
GND	a4	b4	GND
SATA0_RXN	a5	b5	
SATA0_RXP	a6	b6	
GND	a7	b7	GND
SATA1_TXP	a8	b8	
SATA1_TXN	a9	b9	
GND	a10	b10	GND
SATA1_RXN	a11	b11	
SATA1_RXP	a12	b12	
GND	a13	b13	GND
	a14	b14	
	a15	b15	
GND	a16	b16	GND
	a17	b17	
	a18	b18	
+3.3V_SATA	a19	b19	+3.3V_SATA
	a20	b20	
	a21	b21	
+5V_SATA	a22	b22	+5V_SATA
	a23	b23	
	a24	b24	
+12V_SATA	a25	b25	*+12V_SATA*

Notes:

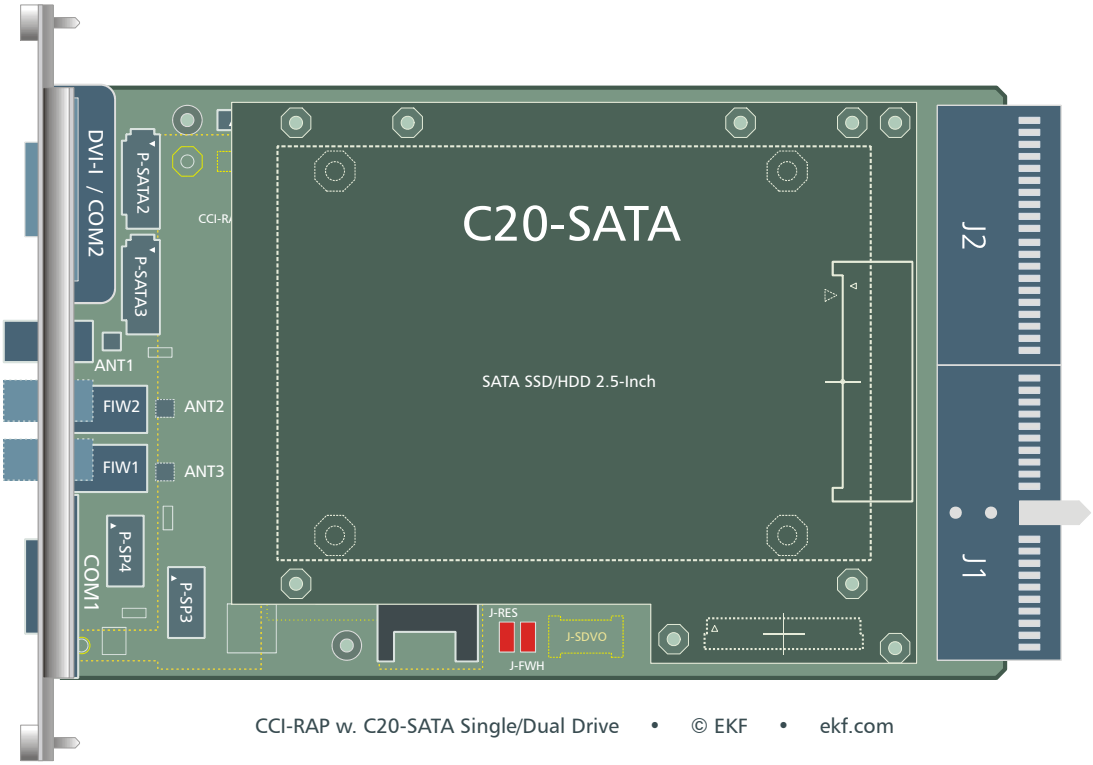
+3.3V_SATA is not connected by default - can be tied to either +3.3V_CR or +3.3V_EXT as stuffing option

+5V_SATA by default is connected to +5V_CR across 1.5A PolySwitch resettable fuse - can be tied to +5V_EXT as stuffing option

All sx pins (shield) are tied to GND

CCI-RAP with C20-SATA (Dual Drive) 10/12HP Assembly

CCI-RAP with C20-SATA (Single Drive) 8HP Assembly

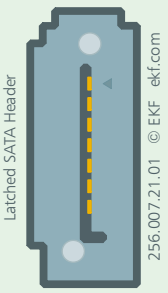


CCI-RAP w. C20-SATA Single/Dual Drive • © EKF • ekf.com

P-SATA2 P-SATA3

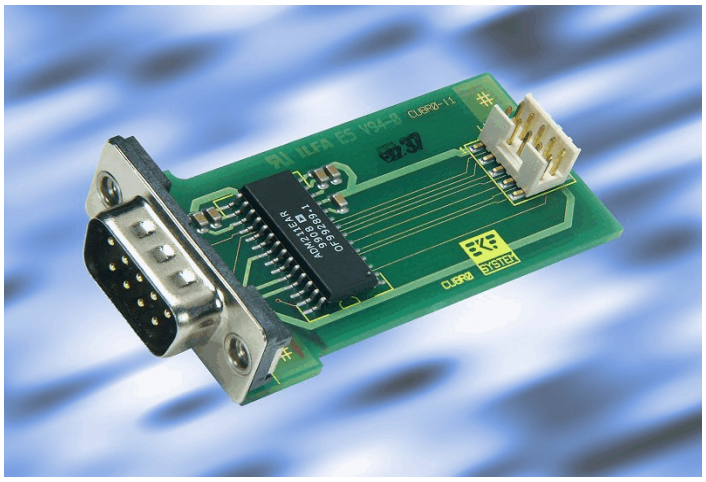
The CCI-RAP can be optionally stuffed with two vertical latched SATA signal headers. TX/RX designation of signals is with respect to the SATA controller. P-SATA2 corresponds to the SATA channel 0 of the JMB363 controller, and P-SATA3 is wired to the JMB363 SATA channel 1.

Usage of P-SATA2/3 is available only exclusive to P-SATA1 and rear I/O SATA via J1 - discuss your actual needs with sales@ekf.de before ordering. Mixed stuffing of P-SATA1 (single channel SATA operation) and either one of P-SATA2 or P-SATA3 is also an option.

P-SATA2 P-SATA3 #256.007.21.01 Latched Headers		
	1	GND
	2	SATA_TX+
	3	SATA_TX-
	4	GND
	5	SATA_RX-
	6	SATA_RX+
	7	GND

P-SP3 P-SP4

The on-board SIO (Super I/O controller) provides up to four serial interfaces (UART, DOS COM ports). While the serial ports SP1 und SP2 have dedicated RS-232 transceivers on-board and are available as COM-A and COM-B from the front panel, another set of two UARTs has been wired to the optional pin headers P-SP3 and P-SP4 (TTL-level). P-SP3 and P-SP4 are suitable for attachment of EKF CU-series PHY modules via a micro ribbon flat cable assembly. A PHY module is a transceiver from TTL level signals to a specific symmetric or asymmetric interface standard, e.g. EIA-485 or RS-232E, with or w/o galvanic isolation. Please contact sales@ekf.de for availability of different CU-series modules (inquiries for custom specific PHY or transition modules welcome). Also custom specific front panel design can be done.



CU-Series PHY Module

Due to another (primary) SIO typically available on the CCG-RUMBA host board, the serial interfaces are not necessarily assigned to COM-1/COM-4 by the operating system. Verify or modify the accompanying CCG-RUMBA BIOS settings for mapping of physical asynchronous serial I/O ports to the logical COM port order.

Alternatively the connectors P-SP3 and/or P-SP4 can be used as 5V tolerant programmable I/O. Details can be derived from the SCH3114 Super I/O controller data sheet (www.smsc.com).

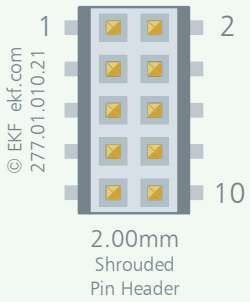
In addition, the serial ports 3 and 4 are also available for rear I/O across J1 (option). In order to avoid signal interference, attach a transceiver module either on-board to P-SP3/4, or on the rear I/O transition module, but not both.

There are two signal pairs, which may be in use as GPO for alternate purposes:

1. SP3_DTR# can be configured (stuffing option) as WDIS_MC1# (wireless turn off, P-PEMC1 Mini Card 1), and likewise acts SP3_RTS# as WDIS_MC2#, P-PEMC2. Not in use by default.

2. SP4_DTR# can be configured (stuffing option) as SMBus EEPROM address line A1, and SP4_RTS# can be configured as SMBus EEPROM Write Protect WP. Not in use by default.

P-SP3 TTL-Level Serial I/O or GPIO 2.00mm Pin Header 2 x 5 (277.01.010.21)



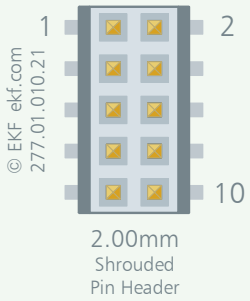
2.00mm Shrouded Pin Header

+5V_SP3 0.5A [1]	1	2	DSR3# / GP12
RI3# / GP13	3	4	RXD3 / GP10
TXD3 / GP11	5	6	DTR3# / GP15 *
RTS3# / GP17 *	7	8	CTS3# / GP16
DCD3# / GP12	9	10	GND

[1] short circuit protection by a PolySwitch resettable fuse, voltage derived from +5V_CR carrier board switched power well

* WDIS_MC1# can be optionally (stuffing option) controlled by SIO GP15 (serial port 3 DTR#), WDIS_MC2# is likewise tied to GP17 (serial port 3 RTS#).

P-SP4 TTL-Level Serial I/O or GPIO 2.00mm Pin Header 2 x 5 (277.01.010.21)



2.00mm Shrouded Pin Header

+5V_SP4 0.5A [1]	1	2	DSR4# / GP66
RI4# / GP31	3	4	RXD4 / GP64
TXD4 / GP65	5	6	DTR4# / GP34 **
RTS4# / GP67 **	7	8	CTS4# / GP62
DCD4# / GP63	9	10	GND

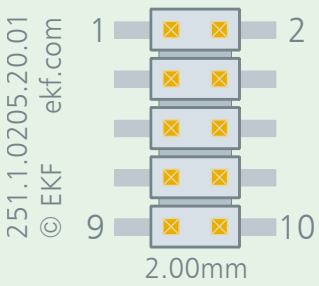
[1] short circuit protection by a PolySwitch resettable fuse, voltage derived from +5V_CR carrier board switched power well

** SMBus EEPROM A1 can be optionally controlled (stuffing option) by SIO GP34 (serial port 4 DTR#), SMBus EEPROM WP is likewise tied to GP67 (serial port 4 RTS4#)

P-UFD1 P-UFD2

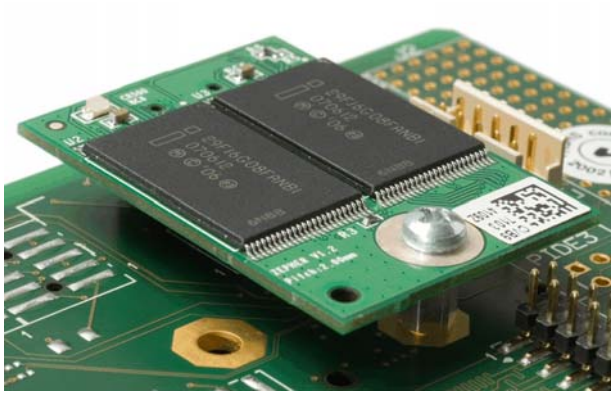
As an option, the CCI-RAP can be equipped with a connector for an industrial style USB Flash disk mezzanine module. The connector is a 2.0mm pitch pin header, suitable for a low profile SSD (Solid-State Drive) 37mm x 26mm. As of current, such modules are available e.g. from M-Systems, STEC, Intel, SanDisk and other manufacturers, up to 8GByte.

P-UFD ○ 2.00mm Pin Header 2x5 (251.1.0205.20.01)
USB Solid-State Drive (Low Profile) 562.20.0004.00 (4GB)
M-Systems uDOC MD1675 • SimpleTech SLUFDM • Intel Z-U130 SSDUSMS • SanDisk SDUS5EB



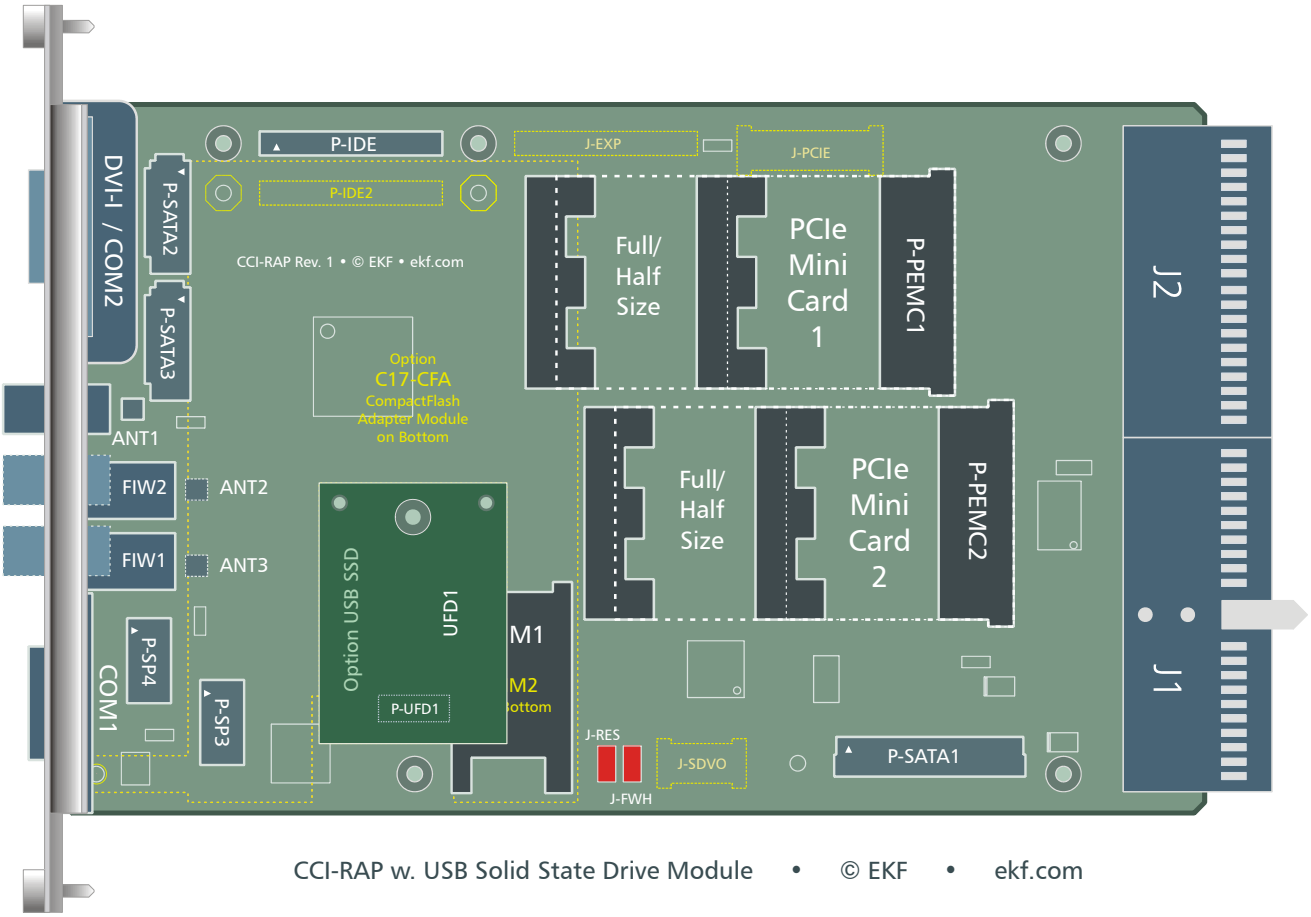
+5V_CR	1	2	NC
USB+	3	4	NC
USB-	5	6	NC
GND	7	8	NC
Mech. Key	9	10	NC

Unfortunately, the CCI-RAP receives 2 USB channels from the CCG-RUMBA, but provides 3 potential USB target devices. Besides the USB Flash disk module optional connector P-UFD, there are the P-PEMC1/2 Mini Card connectors on the CCI-RAP as potential USB devices. The P-UFD shares its USB port with the P-PEMC2 connector. A set of zero Ohm resistors can be stuffed to assign this USB channel either to P-PEMC2 or P-UFD. Thus, if P-UFD is populated, P-PEMC2 does not provide USB connectivity. However, with modern designs such as the Intel® 4965AGN WLAN Mini Card or Intel® Turbo Memory attached to P-PEMC2, USB is not required for Mini Card operation (such modules use PCI Express connectivity), so that P-PEMC2 can be used concurrently to P-UFD in many cases.



USB Solid State Drive

As a stuffing option, the connector P-UFD is populated either on top (P-UFD1) or on bottom (P-UFD2) of the CCI-RAP. The top mounting alternate (P-UFD1) is not recommended if in addition the C20-SATA 2.5-inch hard disk mezzanine module is present, since the hard disk extends over the space required for the top mount USB SSD module. Please specify your needs when ordering.



CCI-RAP w. USB Solid State Drive Module • © EKF • ekf.com

SIM1 SIM2

Optional SIM card sockets SIM1/SIM2 on the CCI-RAP are wired to the P-PEMC1/P-PEMC2 Mini Card connectors, for applications which require subscriber identification such as GSM cellular telephone. In addition, the UIM signals of both Mini Cards are also available for rear I/O across J1.

SIM1 SIM2 SIM card socket hinge (top load) 219.51.006.00	
c1	UIM Power
c2	UIM Reset
c3	UIM Clk
c4	nc
c5	GND
c6	UIM Vpp
c7	UIM Data
c8	nc

Both SIM card holders are hinge style sockets. The frame which holds the SIM card must be unlocked by (carefully) moving it sideways, before it can be lifted. Due to limited space on the CCI-RAP PCB, SIM1 and SIM2 may be partly covered by the C20-SATA mezzanine module, which may require a pliers to insert or remove the SIM card.

For applications with need for easy access to the SIM card, usage of the rear I/O option is recommended. On a suitable (custom specific) rear I/O transition module a push/pull style SIM card holder can be easily integrated into the back panel.

On-Board Jumpers

Most options on the CCI-RAP are stuffing options, so there are only 2 jumpers which are available for user interaction, J-RES (force reset) and J-FWH2 (select Firmware Hub).

J-RES Reset

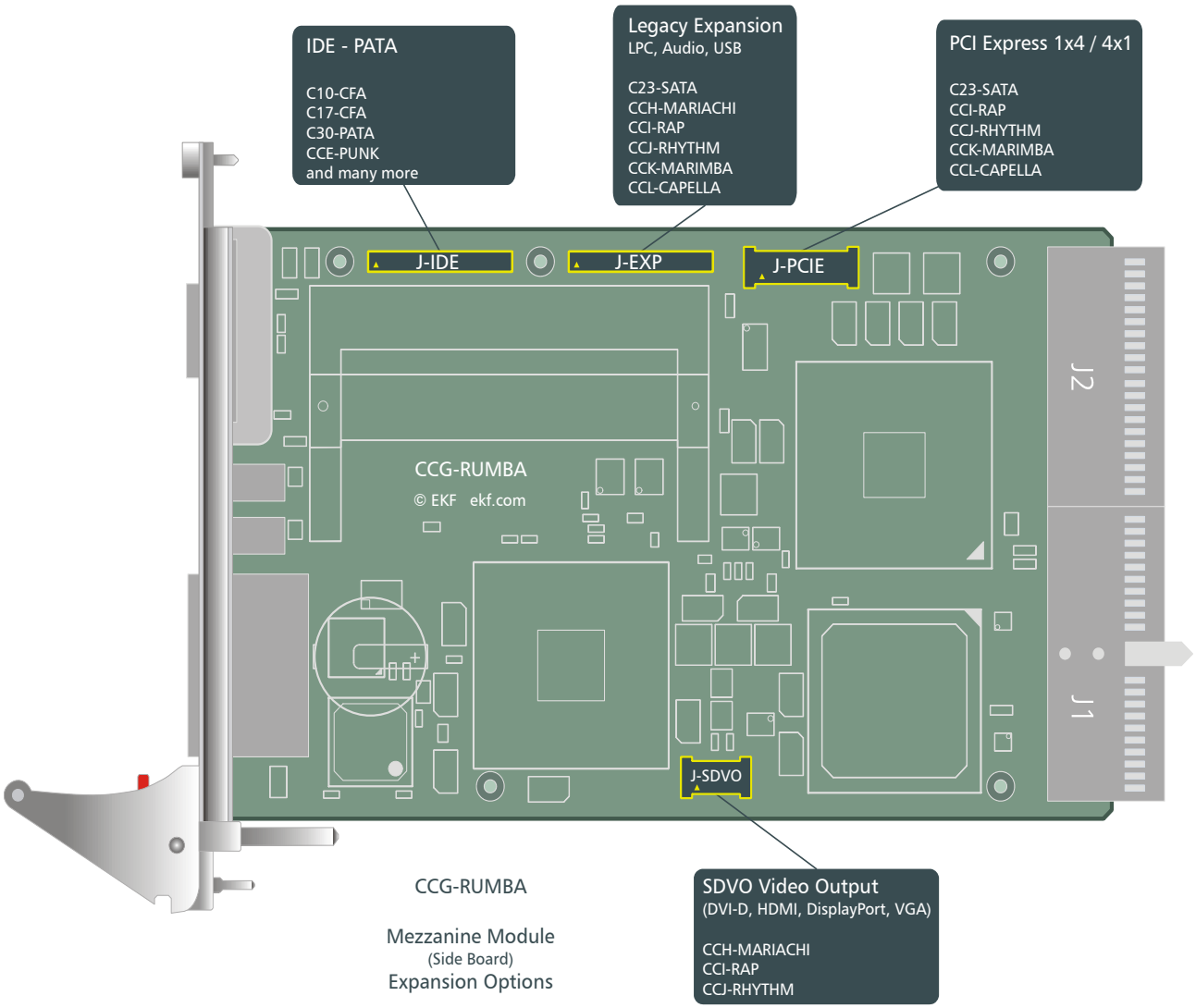
Provided as an option, the pin header J-RES can be used for resetting the CPU host board (processor reset) if wired to additional circuitry (e.g. watchdog or manual pushbutton). Tie reset# to GND with an open collector output. While debugging the system, a 2.54mm jumper may be used to force a manual reset.

J-FWH2

Please see description in chapter 'Firmware Hub 2'.

Inter-Board Connectors

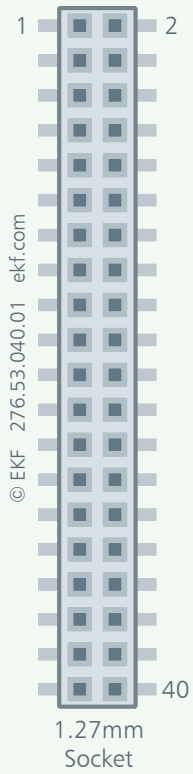
The CCI-RAP is equipped with up to 3 inter-board connectors. These are the P-EXP (LPC and mixed signals), the P-PCIe (4-Link PCI Express), and the P-SDVO, which is available as an option only (if the bord is provided with the video output, i.e. PanelLink transmitter and DVI connector). All inter-board connectors are situated at the bottom of the CCI-RAP and establish the data path and power link to the carrier board CPU. As the CCI-RAP comes typically mounted as a unit together with the CCG-RUMBA, there is normally no need for the user to get access to any of the inter-board connectors. They are described here as a reference only and for better understanding of the CCI-RAP.



Position of Inter-Board Connectors on a CPU Carrier Board

P-EXP

The inter-board connector P-EXP is mounted on bottom of the CCI-RAP PCB, with its face aligned towards the corresponding connector on the CCG-RUMBA. This allows to attach the CCI-RAP mezzanine companion card on top of the CPU carrier board. A suitable board stacker is used in addition to bridge the gap between the two boards. P-EXP is used to pass the Low Pin Count I/F to the CCI-RAP, besides USB channels and other sideband signals.



pin orientation shows
CPU carrier board top view

P-EXP Expansion Board Interface (LPC/HD-Audio/USB) 1.27mm Socket 2 x 20 (276.53.040.01)			
GND	1	2	+3.3V_CR *
CLK_33MHZ	3	4	PLTRST#
LPC_AD0	5	6	LPC_AD1
LPC_AD2	7	8	LPC_AD3
LPC_FRAME#	9	10	LPC_DRQ#
GND	11	12	+3.3V_CR *
SERIRQ	13	14	PME#
SMI#	15	16	CLK_14MHZ
FWH_ID0	17	18	FWH_INIT#
KBD_RST#	19	20	A20GATE
GND	21	22	+5V_CR *
USB_P2N [1]	23	24	USB_P1N [2]
USB_P2P [1]	25	26	USB_P1P [2]
USB_OC# [3]	27	28	DBRESET#
SMB_CLK	29	30	SMB_DAT
GND	31	32	+5V_CR *
PE Port Cfg Bit 1 HDA_SDOUT	33	34	HDA_SDIN0
C-LINK_RST [4] HDA_RST#	35	36	PE Port Cfg Bit 0 HDA_SYNC
C-LINK_CLK [4] HDA_BITCLK	37	38	C-LINK_DAT [4] HDA_SDIN1
SPEAKER	39	40	+12V_CR

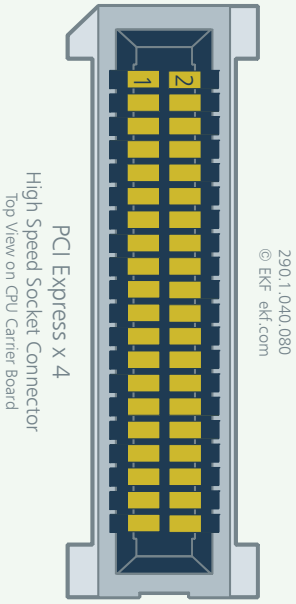
[1] connects to USB Port 6 on CCG-RUMBA
[2] connects to USB Port 5 on CCG-RUMBA
[3] connects to USB_OC56#on CCG-RUMBA
[4] future option WiFi Link for wireless iAMT

* switched power supply lines from CPU carrier board according to Sx state

P-PCIE

The high speed expansion socket P-PCIE is mounted on bottom of the CCI-RAP. This allows to attach the mezzanine companion card on top of the CPU carrier board. A mating strip line PCB (C22-PCIEX2) is used in addition to bridge the gap between the two boards, which results from the horizontal 0.8-inch (20.32mm) card slot pitch. P-PCIE is organized as 4 single PCIe lanes on the CCI-RAP.

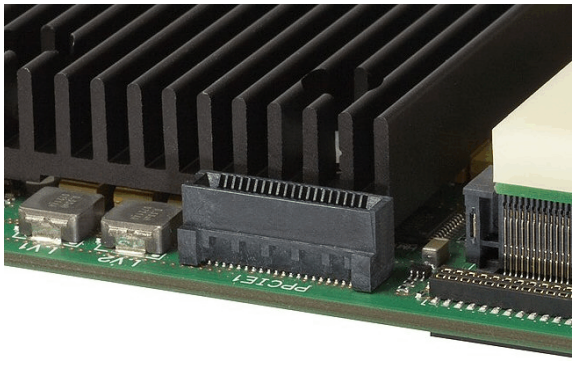
P-PCIE PCI Express x 4 High Speed Dual Row Socket 0.8mm Pitch 290.1.040.080



pin orientation shows CPU carrier board top view (see-trough CCI-RAP PCB)

[1] switched on/off power lines on CCG-RUMBA CPU carrier board according to S3 state

GND	1	2	GND
+5V_CR [1]	3	4	+3.3V_CR [1]
+5V_CR [1]	5	6	+3.3V_CR [1]
GND	7	8	GND
PE_CLKP	9	10	PE_RST#
PE_CLKN	11	12	PE_WAKE#
GND	13	14	GND
PE0_TP	15	16	PE0_RP
PE0_TN	17	18	PE0_RN
GND	19	20	GND
GND	21	22	GND
PE1_TP	23	24	PE1_RP
PE1_TN	25	26	PE1_RN
GND	27	28	GND
PE2_TP	29	30	PE2_RP
PE2_TN	31	32	PE2_RN
GND	33	34	GND
PE3_TP	35	36	PE3_RP
PE3_TN	37	38	PE3_RN
GND	39	40	*+12V_CR*

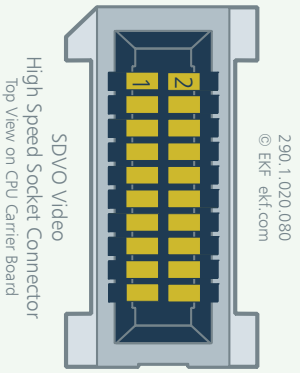


P-PCIE on Carrier Board

P-SDVO

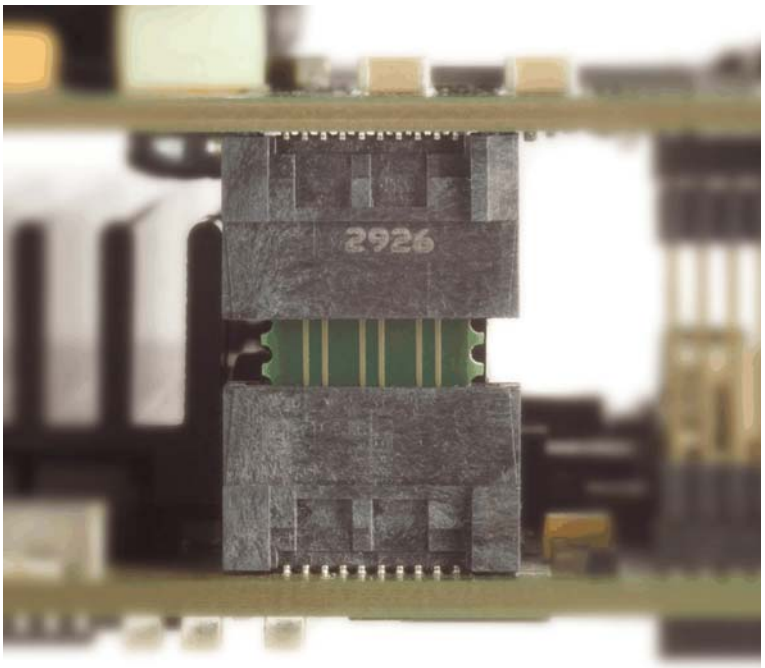
As an option, the high speed expansion socket P-SDVO is mounted on bottom of the CCI-RAP. This allows to attach the mezzanine companion card on top of the CPU carrier board. A mating strip line PCB (C21-PCIEX1) is used in addition to bridge the gap between the two boards, which results from the horizontal 0.8-inch (20.32mm) card slot pitch.

P-SDVO SDVO Video High Speed Dual Row Socket 0.8mm Pitch (290.1.020.080)



pin orientation shows
CPU carrier board top view

GND	1	2	GND
SDVO_RED+	3	4	SDVO_CLK+
SDVO_RED-	5	6	SDVO_CLK-
GND	7	8	GND
SDVO_GREEN+	9	10	SDVO_INT+
SDVO_GREEN-	11	12	SDVO_INT-
GND	13	14	GND
SDVO_BLUE+	15	16	SDVO_CTR_CLK
SDVO_BLUE-	17	18	SDVO_CTR_DATA
GND	19	20	GND

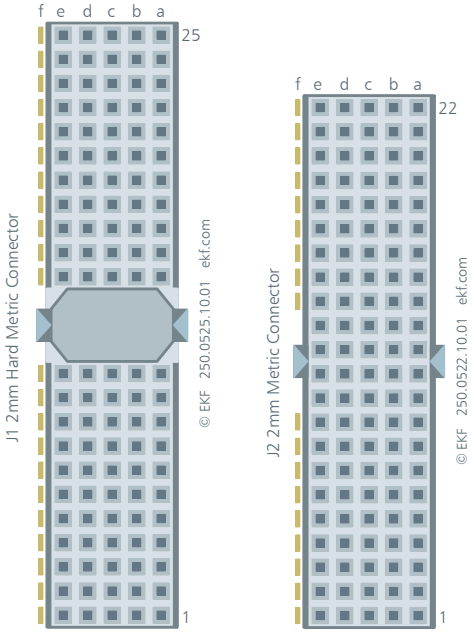


Rear I/O Connectors

J1 J2

As an option, the CCI-RAP can be equipped with the rear I/O connectors J1 and J2. A single slot rear I/O backplane (directly adjoining the CPCI backplane) would be required for handing over the available signal lines to a suitable rear I/O transition module.

The CCI-RAP must not be plugged into a common CPCI slot in order to avoid damaging the board or other components of the system. A brown key on the J1 connector will prevent the user from erroneously inserting the CCI-RAP into an unsuitable position.



Signal names provided on the J1 and J2 connector tables hereafter are associated with their main function. However, the Super I/O controller allows a number of signals also be used as general purpose I/O. Please consult the SMSC SCH3114 datasheet for details (www.smsc.com).

Please note, that the majority of signals is also available on-board or via front panel. Be sure to have connected any signal only once, in order to avoid interference.

#J1	A	B	C	D	E
25	+5V_CR			+3.3V_CR	+5V_CR
24	PEMC2_UIM_C7	GND			
23	PEMC2_UIM_C6	GND			
22	PEMC2_UIM_C3	GND			
21	PEMC2_UIM_C2	GND			
20	PEMC2_UIM_C1	GND			
19	PEMC1_UIM_C7	GND			
18	PEMC1_UIM_C6	GND			
17	PEMC1_UIM_C3	GND			
16	PEMC1_UIM_C2	GND			
15	PEMC1_UIM_C1	GND			
14					
13			KEY (BROWN)		
12					
11	SATA0 TX+	GND			
10	SATA0 TX-	GND			
9	+5V_EXT *	+3.3V_EXT *	GND	*-12V_EXT **	+12V_EXT *
8	SATA0 RX-	GND	GND		
7	SATA0 RX+	GND			
6	GND	GND			
5	SATA1 TX+	GND			
4	SATA1 TX-	GND			
3	GND	GND			
2	SATA1 RX-	GND			
1	SATA1 RX+	GND	GND		

* optional external supply voltages, e.g. for C20-SATA mezzanine (Hard Disk)

#J2	A	B	C	D	E
22	+5V_CR	+3.3V_CR	RSVD	RSVD	+12V_CR
21	GND	GND	GND	GND	GND
20	SP1_RI#	SP1_CTS#	SP2_RI# / GP50	SP2_CTS# / GP56	RSVD
19	SP1_RXD	GND	SP2_RXD / GP52	GND	FWH_GPI1
18	SP1_DSR#	SP1_DCD#	SP2_DSR# / GP54	SP2_DCD# / GP51	FWH_GPI2
17	SP1_DTR#	GND	SP2_DTR# / GP57	GND	GND
16	SP1_RTS#	SP1_TXD	SP2_RTS# / GP55	SP2_TXD / GP53	DBRESET#
15	RSVD	GND	RSVD	GND	RSVD
14	SP3_RI# / GP13	SP3_CTS# / GP16	SP4_RI# / GP31	SP4_CTS# / GP62	SMB_DAT 1)
13	SP3_RXD / GP10	GND	SP4_RXD / GP64	GND	SMB_CLK 1)
12	SP3_DSR# / GP14	SP3_DCD# / GP12	SP4_DSR# / GP66	SP4_DCD# / GP63	GND
11	SP3_DTR# / GP15	GND	SP4_DTR# / GP34 2)	GND	USB1_D-
10	SP3_RTS# / GP17	SP3_TXD / GP11	SP4_RTS# / GP67 2)	SP4_TXD / GP65	USB1_D+
9	RSVD	GND	RSVD	GND	GND
8	LPT_SLCT	LPT_PE	LPT_BUSY	SIO_GP47	USB_OC#
7	LPT_ACK#	GND	GND	SIO_GP46	GND
6	LPT_D7	LPT_D6	LPT_D5	SIO_GP45	USB2_D-
5	LPT_D4	GND	LPT_D3	SIO_GP44	USB2_D+
4	LPT_D2	LPT_D1	LPT_SLCTIN#	SPEAKER	GND
3	LPT_D0	GND	LPT_INIT#	KBDAT	KBCLK
2	LPT_ALF#	LPT_ERROR#	LPT_STROBE#	GND	+5V_CR
1	GND	GND	GND	MSDAT	MSCLK

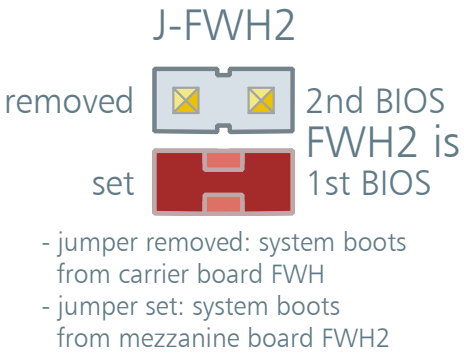
1) stuffing option: SM Bus signals buffered via LTC4300A-3, voltage level @ +5V_CR
buffer enable input is controlled by GP40 SCH3114 SIO (high=enabled)

2) GP34 may be used to control serial EEPROM A1 (stuffing option)
GP67 may be used to control serial EEPROM WP (stuffing option)

Additional Functions

Firmware Hub 2

The CCI-RAP is optionally provided with a 82802 compatible 8Mbit Flash (Firmware Hub), which can be used either as alternative boot BIOS, as an expansion memory to the CPU board BIOS, or for BIOS retrieval/rescue. The Firmware Hub is connected to the LPC (Low Pin Count) interface. The device ID of a particular FWH determines whether it is detected as BIOS after power on (ID = 0). If stuffed, the jumper J-FWH sets the on-board FWH2 ID to zero (and simultaneously changes the CCG-RUMBA SPI Flash BIOS ID to 1) - hence the system will use the BIOS on the CCI-RAP after power-on.



A programming tool for the Firmware Hub and latest BIOS releases can be obtained from the EKF website.

SMBus EEPROM

The CCI-RAP is provided with a 24C01 1Kbit I^2C EEPROM, for storing board configuration data. The EEPROM is accessed via the SMBus. If there is need for storing additional customer data, EKF can place an EEPROM instead with custom specific data space, e.g. 24C16.

If required, the SMBus EEPROM A1 can be optionally controlled (stuffing option) by SIO GP34 (serial port 4 DTR#), and the SMBus EEPROM WP is likewise tied to GP67 (serial port 4 RTS4#).

Trusted Platform Module

The CCI-RAP can be optionally equipped with a Trusted Platform Module cryptographic chip according to the TPM 1.2 specification. The board provides a footprint which is suitable for

- SLB9635 (Infineon www.infineon.com/tpm)
- AT97SC3203 (Atmel www.atmel.com)

and other brands. The TPM chip communicates with the CPU carrier board through the LPC interface. Recent operating systems such as Windows Vista and Linux provide TPM software support.

Typically, TPM chip manufacturers provide the necessary device driver software for integration into special operating systems, along with BIOS drivers. Full documentation for TCG primitives can be found in the TCG TPM Main Specification, Parts 1 – 3, on the TCG website located at https://www.trustedcomputinggroup.org/. TPM features specific to PC Client platforms are specified in the "TCG PC Client Specific TPM Interface Specification, Version 1.2", also available on the TCG web site. Implementation guidance for 32-bit PC platforms is outlined in the "TCG PC Client Specific Implementation Specification for Conventional BIOS for TCG Version 1.2", also available on the TCG web site.

Atmels TPM includes a cryptographic accelerator capable of computing a 2048-bit RSA signature in 500 ms and a 1024-bit RSA signature in 100ms. Performance of the SHA-1 accelerator is 50us per 64-byte block. TCG key generation operations will be completed using a proprietary mechanism in less than 1 msec. The TPM is offered to OEM manufacturers as a turnkey solution, including the firmware integrated on the chip.

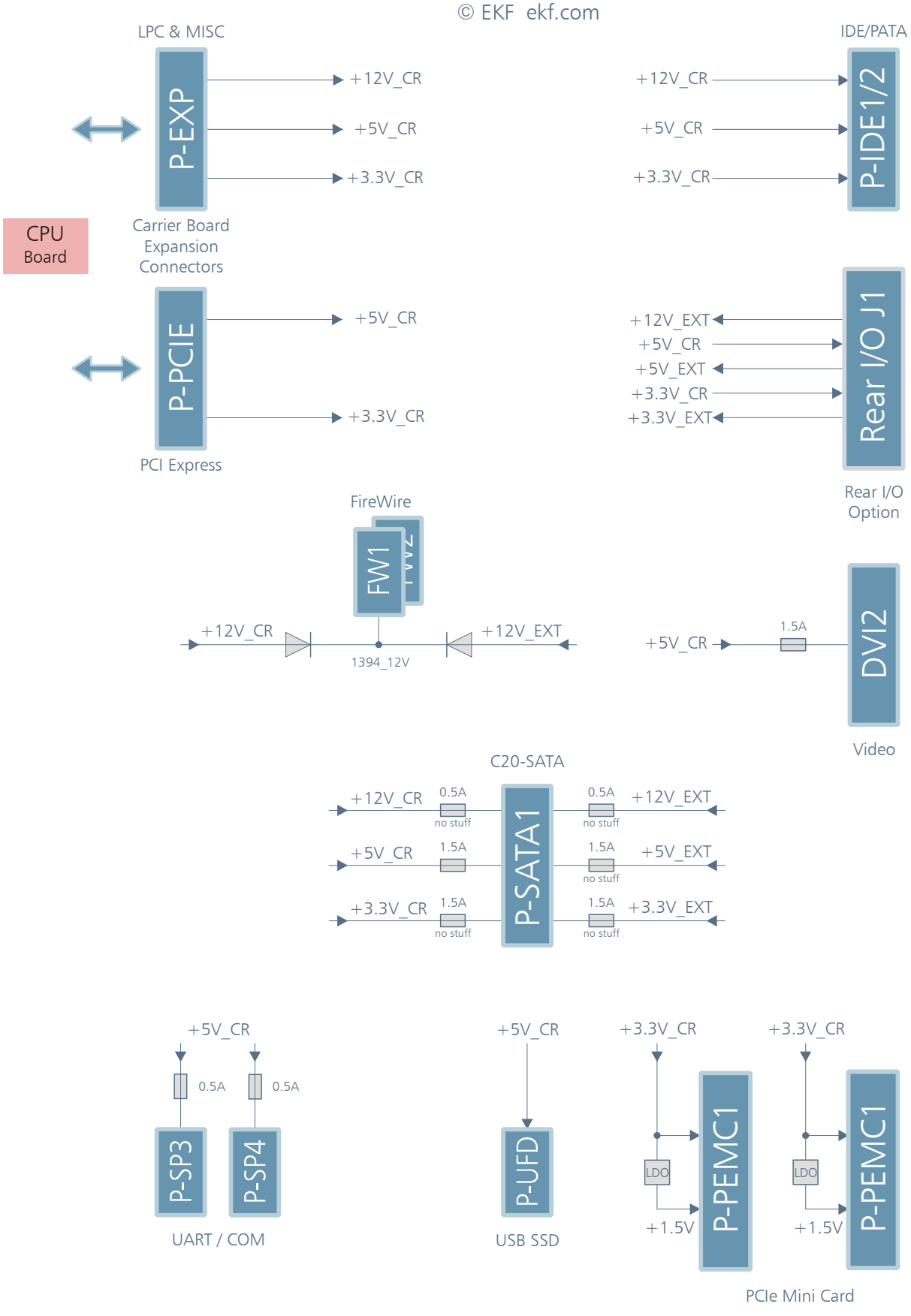
Infineons security controllers have achieved the industry's highest rating for digital security, the Common Criteria EAL 5 high Certificate issued by the German government agency responsible for security in information technology. Infineon provides OEMs with a complete TCG solution that includes all required hardware, software, and management utilities to develop a complete platform security solution.

Power Distribution

The CCI-RAP gets its power from two sources: The CPU carrier board supplies +3.3V_CR, +5V_CR, and +12V_CR, which may be switched off according to the current system sleep state. In addition, the rear I/O connector J1 can also be used to deliver alternate power to the SATA drives (+5V_EXT, +3.3V_EXT), and to the FireWire front panel connectors (+12V_EXT).

For the C20-SATA hard disk drive mezzanine module, the +5V power source can be selected by a Polyswitch resettable fuse (stuffing option) between +5V_CR and +5V_EXT. The 1394 +12V bus power is derived concurrently from both, the carrier board +12V_CR, and the J1 +12V_EXT (back-driving protection by Schottky diodes).

Power Distribution
CCI-RAP



Schematics

Complete circuit diagrams for this product are available for customers on request. Signing of a non-disclosure agreement would be needed. Please contact sales@ekf.de for details.

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